

Projekat iz predmenta Projektovnje pomoću računara - Optimizacija konkurentnog koda

Profesor: dr Miloš Stojanović

Studenti:

Ilić Dragana REr 23/13

Nikolić Stefan SEr 56/13

Đurović Igor REr 19/13

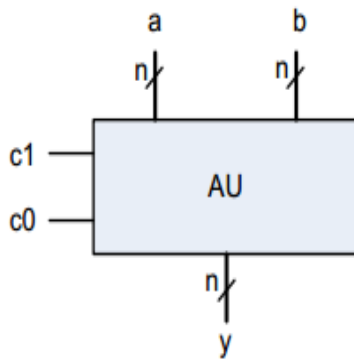


Optimizacija konkurentnog koda

- Cilj: sa što manje hardverskih resursa realizovati željenu funkciju.
- Minimizacija broja aritmetičkih i relacionih operatora u kodu.
- Dve tehnike:
 1. Deoba operatora - preurediti kod tako da se isti operator može iskoristiti za obavljanje više različitih operacija.
 2. Deoba funkcija - više funkcija realizuju se tako da dele neke zajedničke delove ili se jedna funkcija koristi za realizaciju neke druge funkcije.

Zadatak

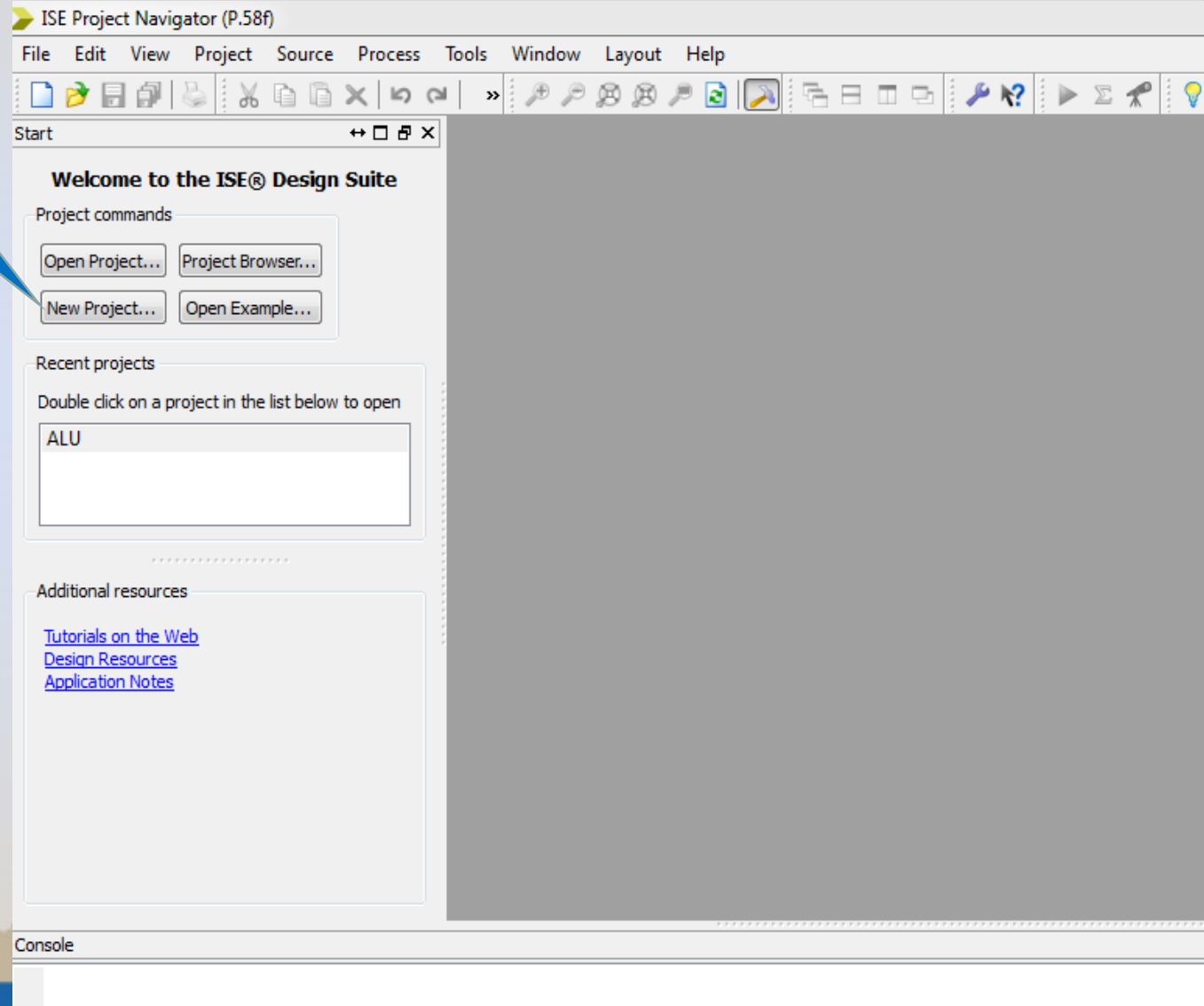
Izvršiti implementaciju dve varijante VHDL opisa višefunkcionalne aritmetičke jedinice na FPGA. Uporediti dva rešenja prema složenosti (zauzeće hardverskih resursa) i performansama (propagaciono kanjenje) za 3 vrednosti gneričkog parametra n : 4, 8 i 16.



c1	c0	Operacija	y
0	0	Sabiranje	$a + b$
0	1	Oduzimanje	$a - b$
1	0	Minimum	$\text{Min}(a, b)$
1	1	Maksimum	$\text{Max}(a, b)$

Početak

Biramo New Project za novi projekat.



Kreiranje novog projekta

New Project Wizard

Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name: au

Location: D:\projekat\au

Working Directory: D:\projekat\au

Description:

Select the type of top-level source for the project

Top-level source type: HDL

More Info Next Cancel

1



2



3



4



1. Upišite ime projekta.
2. Izaberite lokaciju gde će biti smešten.
3. Izaberite tip projekta. (birmo HDL)
4. NEXT



Izbor integrisanog kola

Biramo konkretno kolo za koje će biti realizovan projekat.

Ostalo ostaviti kako jeste, zatim potvrditi sa Next.

New Project Wizard

Project Settings

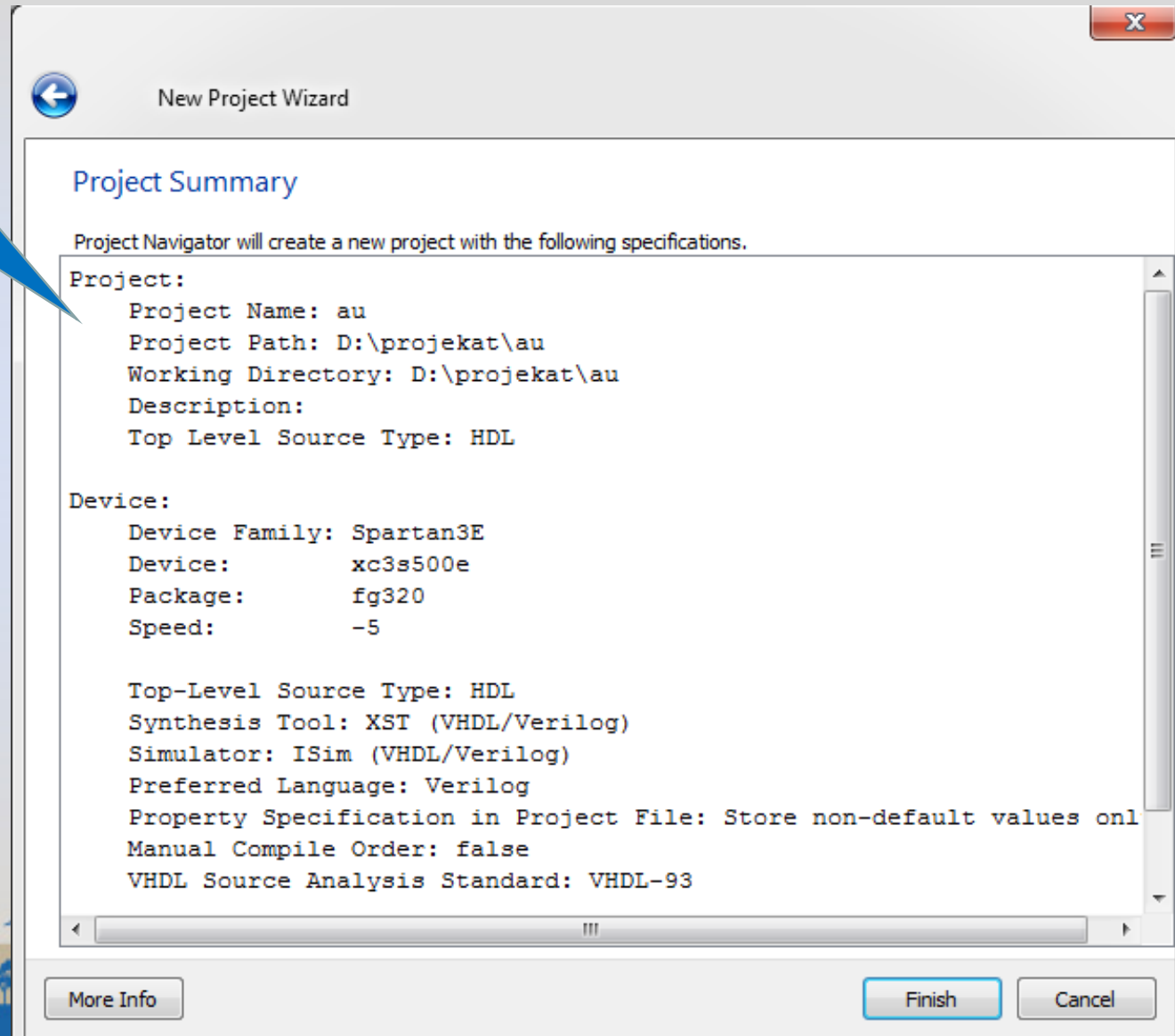
Specify device and project properties.
Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	General Purpose
Family	Spartan3E
Device	XC3S500E
Package	FG320
Speed	-5
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store non-default values only
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

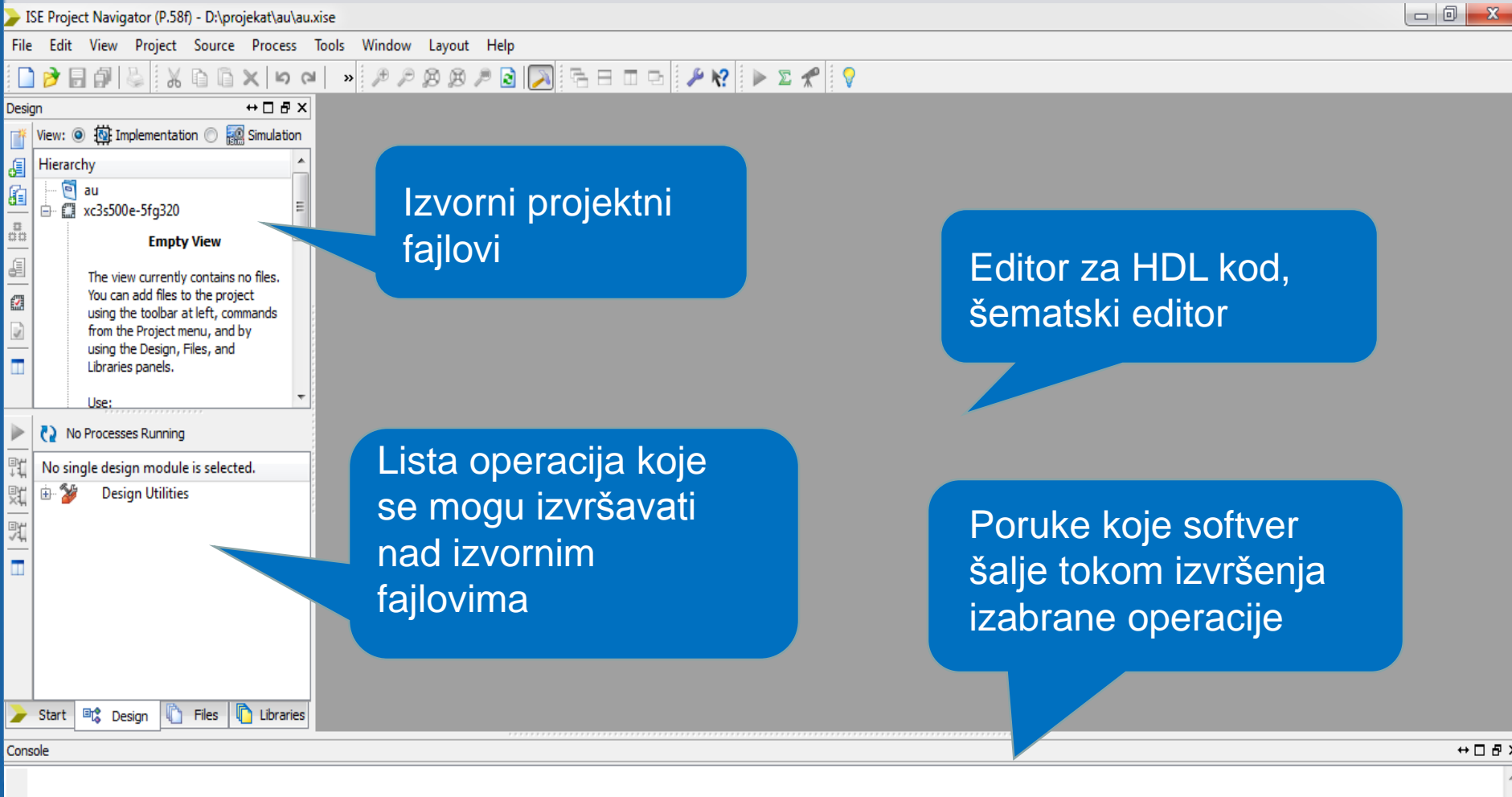
More Info Next Cancel

Rezime projekta

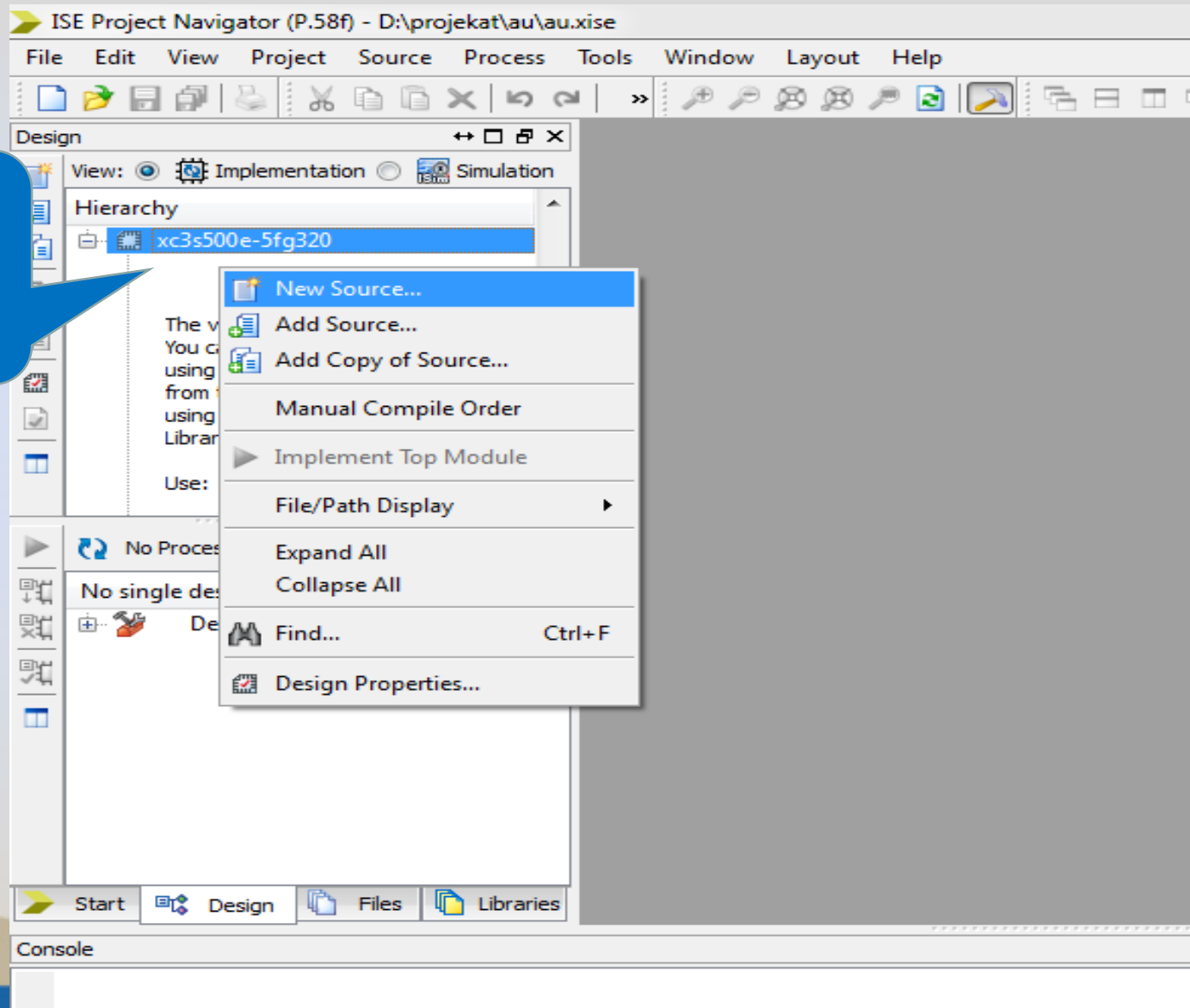
Informativni dijalogo projektu, biramo Finish.



Izgled novog projekta



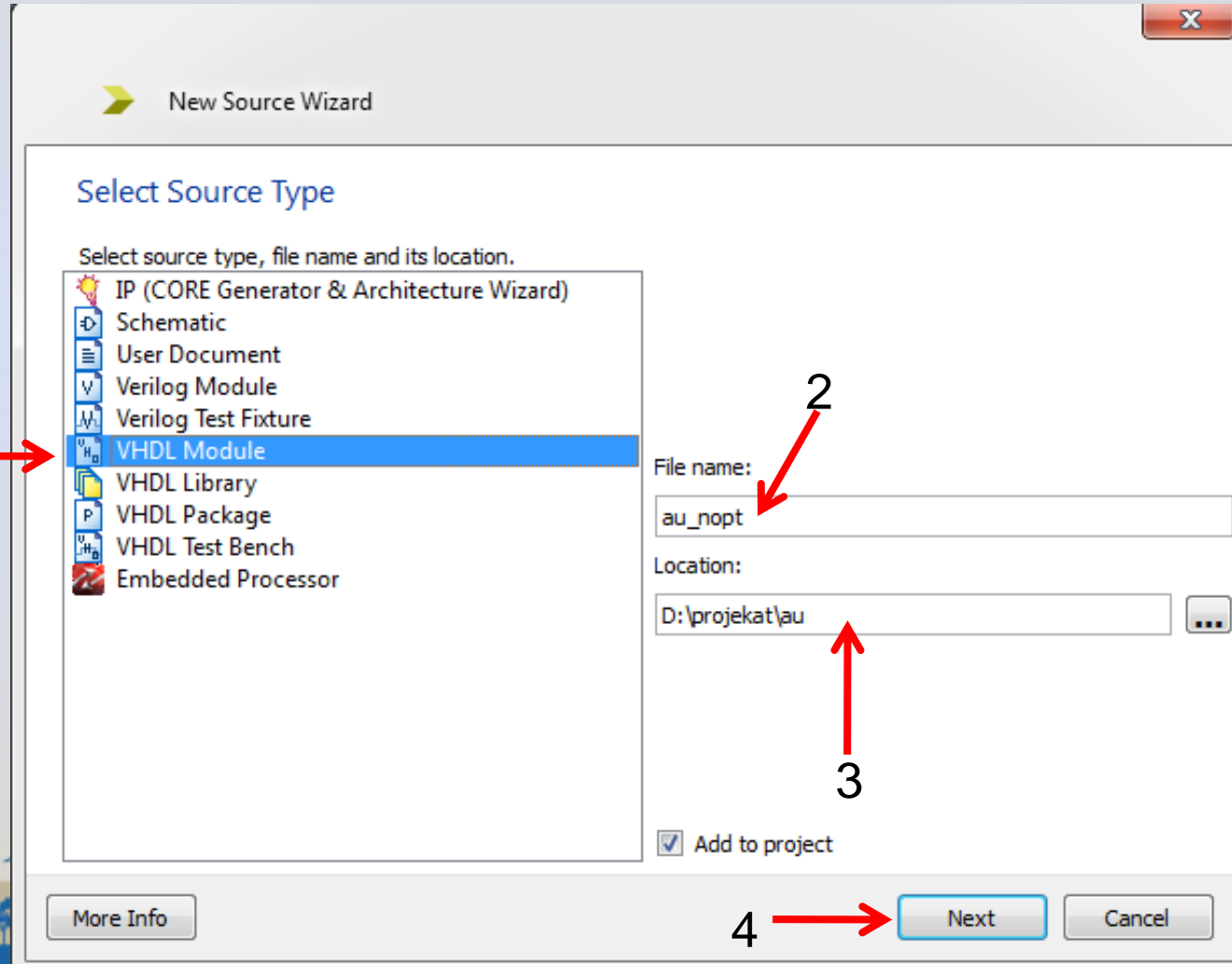
Kreiranje novog projektnog fajla - neoptimizovan kod



Desni klik preko oznake kola, a onda New Source

Kreiranje novog projektnog fajla

1. Izbor tipa projektnog fajla (bira se VHDL Module)
2. Upišite ime projektnog fajla (neka bude au_nopt)
3. Lokacija - neka ostane predložena lokacija
4. Next



“Prazan” modul

1. Next

New Source Wizard

Define Module

Specify ports for module.

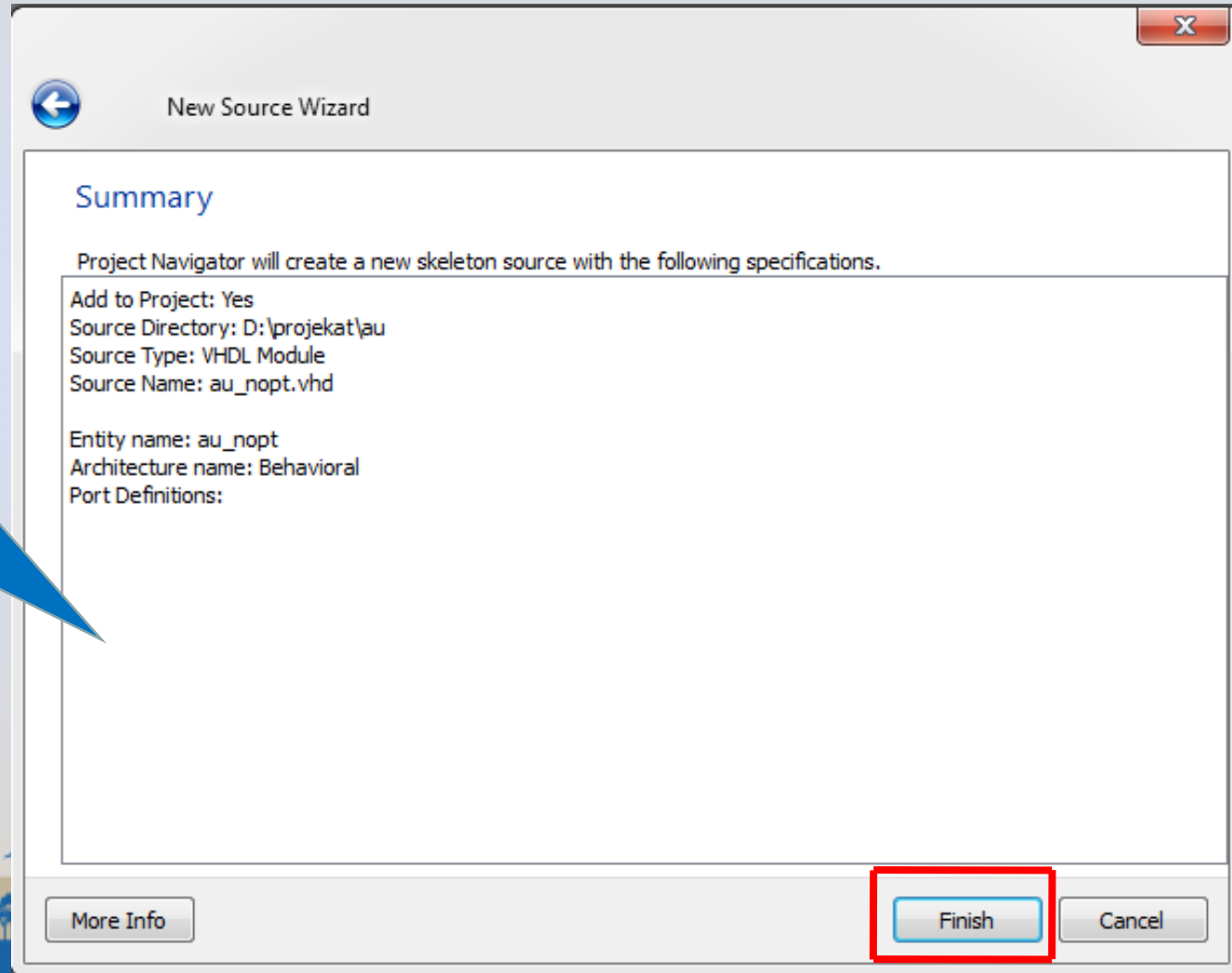
Entity name

Architecture name

Port Name	Direction	Bus	MSB	LSB
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		

More Info

“Prazan” modul



Informativni dijalog o projektnom fajlu, biraemo Finish.



Novi modul - neoptimizovan

Selektovan je projektni fajl.

The screenshot shows the ISE Project Navigator interface. In the Hierarchy pane on the left, the file 'au_nopt - Behavioral (au_nopt.vhd)' is selected. The main editor displays the following VHDL code:

```
1 -----  
2 -- Company:  
3 -- Engineer:  
4 --  
5 -- Create Date:    10:45:21 02/12/2015  
6 -- Design Name:  
7 -- Module Name:    au_nopt - Behavioral  
8 -- Project Name:  
9 -- Target Devices:  
10 -- Tool versions:  
11 -- Description:  
12 --  
13 -- Dependencies:  
14 --  
15 -- Revision:  
16 -- Revision 0.01 - File Created  
17 -- Additional Comments:  
18 --  
19 -----  
20 library IEEE;  
21 use IEEE.STD_LOGIC_1164.ALL;  
22  
23 -- Uncomment the following library declaration if using  
24 -- arithmetic functions with Signed or Unsigned values  
25 --use IEEE.NUMERIC_STD.ALL;  
26  
27 -- Uncomment the following library declaration if instantiating  
28 -- any Xilinx primitives in this code.
```

A blue speech bubble on the right contains the text: 'Obrišemo sve i pišemo kod iz početka'.

Obrišemo sve i pišemo kod iz početka

Pisanje neoptimizovanog koda

The screenshot shows the Xilinx ISE Project Navigator interface. The main window displays a VHDL file named `au_nopt.vhd` with the following code template:

```
1
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    10:45:21 02/12/2015
6  -- Design Name:
7  -- Module Name:    au
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.1 - File Created
17 -- Additional Comments:
18 --
19
20
21
```

A blue callout bubble with white text is positioned over the code, pointing to the area between lines 12 and 19. The text inside the bubble reads: "Ovde pišemo naš kod." (Here we write our code.)

The interface also shows a Hierarchy pane on the left with the project structure, a Processes pane with a list of tasks like "Design Summary/Reports" and "Synthesize - XST", and a Console pane at the bottom with the message "Launching Design Summary/Report Viewer...".

Neoptimizovana arhitektura - kod

Prilikom sisteze koda biće usvojena ova vrednost generičnog parametra

```
18  --
19  -----
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.NUMERIC_STD.ALL;
23
24  entity au is
25      generic (N : integer :=16);
26      port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNT0 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNT0 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNT0 0));
29  END au;
30
31  architecture Behavioral OF au IS
32      SIGNAL sum, dif, min, max : STD_LOGIC_VECTOR(N-1 DOWNT0 0);
33  BEGIN
34      sum <= STD_LOGIC_VECTOR(SIGNED(a) + SIGNED(b));
35      dif <= STD_LOGIC_VECTOR(SIGNED(a) - SIGNED(b));
36      min <= a WHEN (SIGNED(a) < SIGNED(b)) ELSE
37           b;
38      max <= a WHEN (SIGNED(a) > SIGNED(b)) ELSE
39           b;
40      WITH c SELECT
41          y <= sum WHEN "00",
42              dif WHEN "01",
43              min WHEN "10",
44              max WHEN OTHERS;
45  END Behavioral;
```

numeric_std

Podrazumeva vrednost generičnog parametra

Neoptimizovana arhitektura



Pisanje koda

The screenshot displays the Xilinx ISE Project Navigator interface. The main window shows the VHDL source code for a behavioral model of a 16-bit signed adder/subtractor. The code includes library declarations for IEEE, entity and architecture definitions, and logic for calculating sum, difference, and maximum/minimum values based on the sign of the inputs.

```
18  --
19  -----
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.NUMERIC_STD.ALL;
23
24  entity au is
25    generic (N : integer :=16);
26    port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNT0 0);
27          c : IN STD_LOGIC_VECTOR(1 DOWNT0 0);
28          y : OUT STD_LOGIC_VECTOR(N-1 DOWNT0 0));
29  END au;
30
31  architecture Behavioral OF au IS
32    SIGNAL sum, dif, min, max : STD_LOGIC_VECTOR(N-1 DOWNT0 0);
33  BEGIN
34    sum <= STD_LOGIC_VECTOR(SIGNED(a) + SIGNED(b));
35    dif <= STD_LOGIC_VECTOR(SIGNED(a) - SIGNED(b));
36    min <= a WHEN (SIGNED(a) < SIGNED(b)) ELSE
37           b;
38    max <= a WHEN (SIGNED(a) > SIGNED(b)) ELSE
39           b;
40    WITH c SELECT
41      y <= sum WHEN "00",
42          dif WHEN "01",
43          min WHEN "10",
44          max WHEN OTHERS;
45  END Behavioral;
```

The left sidebar shows the project hierarchy with 'au_nopt - Behavioral (au_nopt.vhd)' selected. The bottom console shows the message: "Started : 'Launching ISE Text Editor to edit au_nopt.vhd'. Launching Design Summary/Report Viewer...".

Provera sintakse

Selektovan je projektni fajl.

Klik na + ispred Synthesize -XST

Dvoklik na Check Syntax.

Poruka da nema sintakasnih grešaka

The screenshot displays the ISE Project Navigator interface. The 'Design' window shows the project hierarchy with 'au - Behavioral (au_nopt.vhd)' selected. The 'Processes' window shows the 'Synthesize - XST' process expanded, with 'Check Syntax' checked. The 'Console' window shows the message: 'Entity <au> (Architecture <Behavioral>) compiled. Process "Check Syntax" completed successfully'. The main editor window shows the VHDL code for the 'au' entity, which includes a generic parameter 'N', two input ports 'a' and 'b', and one output port 'y'. The architecture 'Behavioral' implements a full adder circuit using logic vectors and conditional assignments.

```
18 --
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.NUMERIC_STD.ALL;
23
24 entity au is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNT0 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNT0 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNT0 0));
29 END au;
30
31 architecture Behavioral OF au IS
32     SIGNAL sum, dif, min, max : STD_LOGIC_VECTOR(N-1 DOWNT0 0);
33 BEGIN
34     sum <= STD_LOGIC_VECTOR(SIGNED(a) + SIGNED(b));
35     dif <= STD_LOGIC_VECTOR(SIGNED(a) - SIGNED(b));
36     min <= a WHEN (SIGNED(a) < SIGNED(b)) ELSE
37           b;
38     max <= a WHEN (SIGNED(a) > SIGNED(b)) ELSE
39           b;
40     WITH c SELECT
41         y <= sum WHEN "00",
42            dif WHEN "01",
43            min WHEN "10",
44            max WHEN OTHERS;
45 END Behavioral;
```

Implementacija neoptimizovane arhitekture

Selektovan je projektni fajl.

Dvoklik na Implement Design.

Poruka da je implementacija uspešno okončana.

The screenshot displays the Xilinx ISE Project Navigator interface. The 'Design' window shows the project hierarchy with 'au - Behavioral (au_nopt.vhd)' selected. The 'Processes' window shows the implementation steps, with 'Implement Design' highlighted. The 'Console' window at the bottom shows the completion message: 'Process "Generate Post-Place & Route Static Timing" completed successfully'. The main editor window shows the VHDL code for the 'au' entity.

```
18 --
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.NUMERIC_STD.ALL;
23
24 entity au is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNT0 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNT0 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNT0 0));
29 END au;
30
31 architecture Behavioral OF au |IS
32     SIGNAL sum, dif, min, max : STD_LOGIC_VECTOR(N-1 DOWNT0 0);
33 BEGIN
34     sum <= STD_LOGIC_VECTOR(SIGNED(a) + SIGNED(b));
35     dif <= STD_LOGIC_VECTOR(SIGNED(a) - SIGNED(b));
36     min <= a WHEN (SIGNED(a) < SIGNED(b)) ELSE
37           b;
38     max <= a WHEN (SIGNED(a) > SIGNED(b)) ELSE
39           b;
40     WITH c SELECT
41         y <= sum WHEN "00",
42             dif WHEN "01",
43             min WHEN "10",
44             max WHEN OTHERS;
45 END Behavioral;
```

Postavljanje vremenskog ograničenja

Selektovan je projektni fajl.

Klik na + ispred User Constraints

Dupli klik preko "Create Timing Constraints"

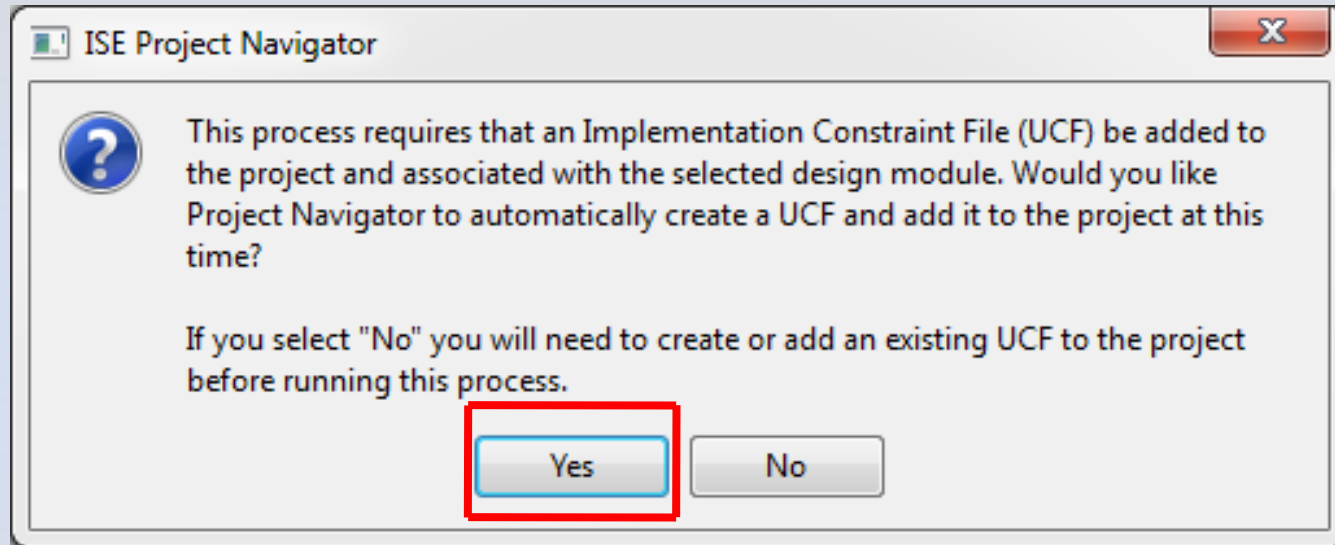
The screenshot displays the Xilinx ISE Project Navigator interface. The top menu bar includes File, Edit, View, Project, Source, Process, Tools, Window, Layout, and Help. The Design window shows the Hierarchy tree with the project file 'au - Behavioral (au_nopt.vhd)' selected. The Processes window shows the 'User Constraints' folder expanded, with 'Create Timing Constraints' highlighted. The VHDL code editor on the right shows the following code:

```
18 --
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.NUMERIC_STD.ALL;
23
24 entity au is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNTO 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNTO 0));
29 END au;
30
31 architecture Behavioral OF au IS
32     SIGNAL sum, dif, min, max : STD_LOGIC_VECTOR(N-1 DOWNTO 0);
33 BEGIN
34     sum <= STD_LOGIC_VECTOR(SIGNED(a) + SIGNED(b));
35     dif <= STD_LOGIC_VECTOR(SIGNED(a) - SIGNED(b));
36     min <= a WHEN (SIGNED(a) < SIGNED(b)) ELSE
37           b;
38     max <= a WHEN (SIGNED(a) > SIGNED(b)) ELSE
39           b;
40     WITH c SELECT
41         y <= sum WHEN "00",
42             dif WHEN "01",
43             min WHEN "10",
44             max WHEN OTHERS;
45 END Behavioral;
```

The Console window at the bottom shows the following output:

```
Total time: 1 secs
Process "Generate Post-Place & Route Static Timing" completed successfully
```

Postavljanje vremenskog ograničenja



Postavljanje vremenskog ograničenja

The screenshot displays the Xilinx ISE Project Navigator interface. The main window is titled "ISE Project Navigator (P.58f) - D:\projekat\au\au.xise - [Timing Constraints]". The menu bar includes File, Edit, View, Project, Source, Process, Tools, Window, Layout, and Help. The toolbar contains various icons for file operations and design actions.

The "Timing Constraints" window is active, showing the "Source Constraint File" set to "auf.ucf". Below this, there are radio buttons for "Show constraints from specified file only" and "Show constraints from all files". The "Save New Constraints To File" is also set to "auf.ucf". The "Constraint Type" list on the left includes UCF Constraints, Timing Constraints (selected), Group Constraints, and Miscellaneous.

A dialog box titled "Project Navigator" is overlaid on the main window, displaying an information icon and the message "The design has no Clocks." with an "OK" button highlighted by a red rectangle.

The bottom status bar shows the "Console" window with the message: "INFO: auf.ucf created and added to project." The taskbar at the bottom includes icons for Start, Timing..., Design, and Design Summary (out of date). The active window is "Timing Constraints".

Postavljanje vremenskog ograničenja

Klik na + ispred
Timing Constraints

Klik na + ispred
Exceptions

Pritisnite desni taster
iznad opcije Paths i
izaberite opciju Create
Constraint.

ISE Project Navigator (P.58f) - D:\projekat\au\au.xise - [Timing Constraints]

File Edit View Project Source Process Tools Window Layout Help

Timing Constraints

Source Constraint File

auf.ucf

Show constraints from specified file only

Show constraints from all files

Save New Constraints To File

auf.ucf

Constraint Type

- UCF Constraints
- Timing Constraints
- Exceptions
 - Path
 - Nets **Create Constraint**
 - Instances and Pins
 - Operating Conditions
 - Group Constraints
 - Miscellaneous

State	TIMESPEC Name	From	Thru	To
1				

Validate Constraints Click "Validate Constraints" button after direct

Start Timing ... Design

Design Summary (out of date)

Console

INFO: auf.ucf created and added to project.

Console Errors Warnings Find in Files Results

Create Constraint

Postavljanje vremenskog ograničenja

The screenshot displays the Xilinx ISE Project Navigator interface with the 'Paths Exceptions' dialog box open. The dialog box is titled 'Paths Exceptions' and contains the following elements:

- Diagram:** A schematic diagram showing a path from a 'FROM group' to a 'TO group' with a 'delay' element in between.
- *TIMESPEC name:** A text field containing 'TS_'.
- Time groups:** Fields for 'From group' and 'To group', each with a 'Create ...' button.
- Through points:** A section with a '+' icon and a 'To group' field with a 'Create ...' button.
- Constraint type:** Radio buttons for 'Explicit' (selected), 'Relative to other path TIMESPEC', and 'Mark as false paths'.
- Explicit settings:** A 'Time' field set to '20' and a 'Units' dropdown set to 'ns'.
- Relative to other path TIMESPEC settings:** A 'Reference TIMESPEC' dropdown, a 'Factor' section with 'Operand' radio buttons for 'Multiply by' (selected) and 'Divide by', and a 'Value' field set to '1'.
- Data path only:** A checkbox labeled 'Data path only' which is currently unchecked.
- Comment:** A text area for entering a comment.
- Buttons:** 'OK', 'Close', 'Create', and 'Help' buttons at the bottom.

The background shows the 'Timing Constraints' window with the 'Source Constraint File' set to 'auf.ucf' and the 'Constraint Type' tree expanded to 'Timing Constraints' > 'Exceptions' > 'Paths'. The console at the bottom shows the message: 'INFO: auf.ucf created and added to project.'

Postavljanje vremenskog ograničenja

Odabrati All Pads.

Odabrati All Pads.

Upisati 20.

Uneti naziv ograničenja, TS_P2P.

Ok.

Paths Exceptions

FROM group — delay — TO group

* TIMESPEC name: TS_P2P

Time groups

From group: All Pads Create ...

Through points: +

To group: All Pads Create ...

Constraint type

Explicit

Time: 20 Units: ns

Relative to other path TIMESPEC

Reference TIMESPEC:

Factor

Operand: Multiply by Divide by

Value: 1

Mark as false paths

Data path only

Comment:

OK Close Create Help

Postavljanje vremenskog ograničenja

State ^	TIMESPEC Name	From	Thru	To	MaxDelay	TIG	Reference TIMESPEC	Factor	Data Path Only	Source
1 OK	TS_P2P	PADS		PADS	20 ns	No			No	au.ucf
2										



Postavljanje vremenskog ograničenja

ISE Project Navigator (P.58f) - D:\projekat\au\au.xise - [Timing Constraints*]

File Edit View Project Source Process Tools Window Layout Help

Timing Constraints

Source Constraint File
au.ucf
 Show constraints from specified file only
 Show constraints from all files

Save New Constraints To File
au.ucf

Constraint Type

- UCF Constraints
 - Timing Constraints
 - Exceptions
 - Paths
 - Nets
 - Instances and Pins
 - Operating Conditions
 - Group Constraints
 - Miscellaneous

Create Timing Constraints for Paths Exceptions (TIG or FROM:TO/MAXDELAY) by direct entry or right click to open context menu

State	TIMESPEC Name	From	Thru	To	MaxDelay	TIG	Reference TIMESPEC	Factor	Data Path Only	Source
1 OK	TS_P2P	PADS		PADS	20 ns	No			No	au.ucf
2										

Project Navigator

Do you want to save the changes you made to: 'D:\projekat\au\au.ucf'?

Validate Constraints Click "Validate Constraints" button after direct entry of any change

Start Timing ... Design au_nopt.vhd Design Summary (out of date) Timing Constraints*

Console

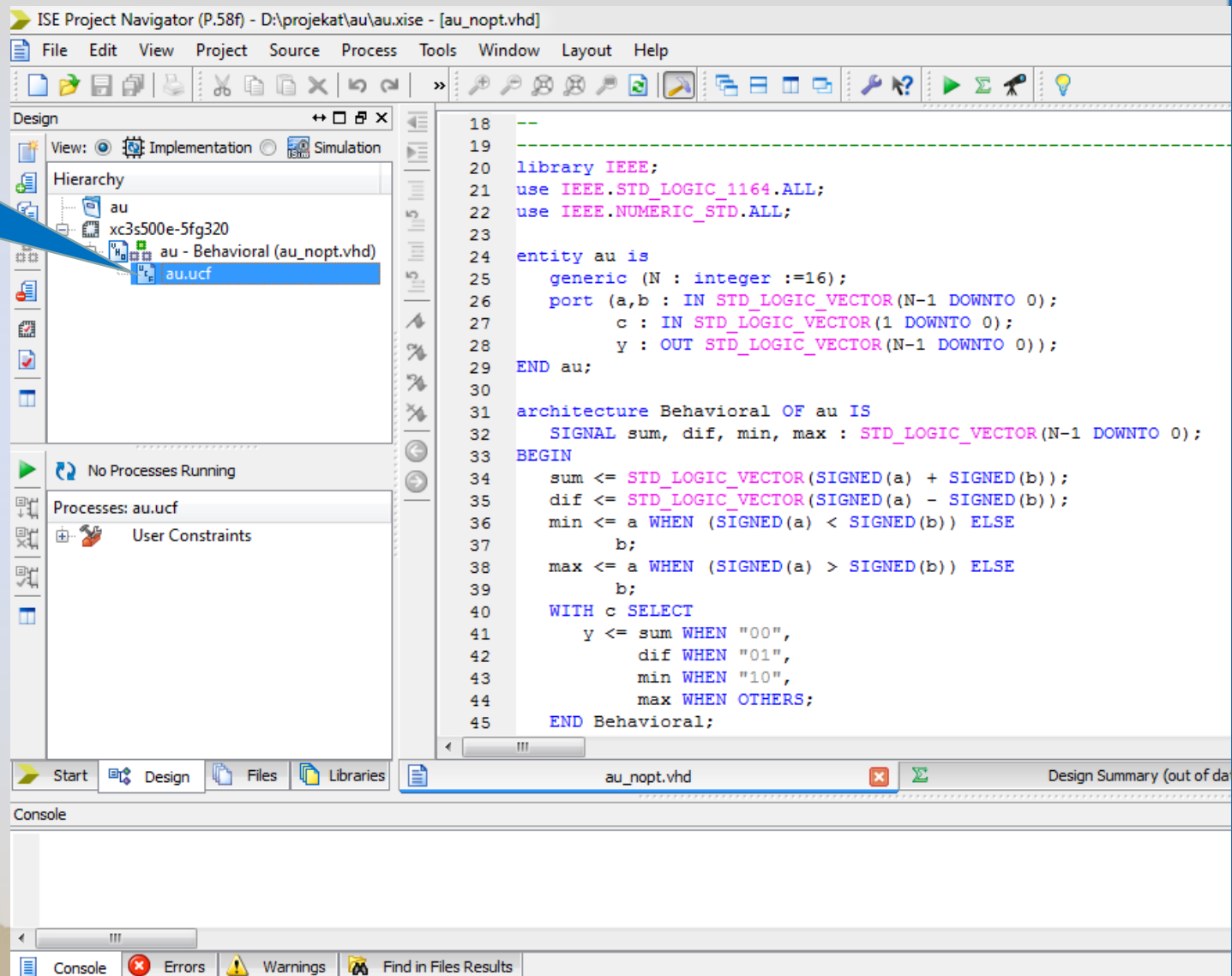
INFO: au.ucf created and added to project.

Console Errors Warnings Find in Files Results



Postavljeno vremensko ograničenje

Kreiran je UCF
fajl.



The screenshot displays the ISE Project Navigator interface. The main window shows a VHDL code editor with the following code:

```
18 --
19 -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.NUMERIC_STD.ALL;
23
24 entity au is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNTO 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNTO 0));
29 END au;
30
31 architecture Behavioral OF au IS
32     SIGNAL sum, dif, min, max : STD_LOGIC_VECTOR(N-1 DOWNTO 0);
33 BEGIN
34     sum <= STD_LOGIC_VECTOR(SIGNED(a) + SIGNED(b));
35     dif <= STD_LOGIC_VECTOR(SIGNED(a) - SIGNED(b));
36     min <= a WHEN (SIGNED(a) < SIGNED(b)) ELSE
37           b;
38     max <= a WHEN (SIGNED(a) > SIGNED(b)) ELSE
39           b;
40     WITH c SELECT
41         y <= sum WHEN "00",
42              dif WHEN "01",
43              min WHEN "10",
44              max WHEN OTHERS;
45 END Behavioral;
```

The left pane shows the Hierarchy view with the following structure:

- View: Implementation
- Simulation
- Hierarchy
 - au
 - xc3s500e-5fg320
 - au - Behavioral (au_nopt.vhd)
 - au.ucf

The bottom pane shows the Console, Errors, Warnings, and Find in Files Results tabs.

Postavljeno vremensko ograničenje

The screenshot shows the ISE Project Navigator interface. The Design Navigator on the left shows the project hierarchy with the file `au.ucf` selected. The main editor window displays the content of `au.ucf`, which is highlighted in a red box. The content is as follows:

```
1  
2 #Created by Constraints Editor (xc3s500e-fg320-5) - 2015/02/12  
3 TIMESPEC TS_P2P = FROM "PADS" TO "PADS" 20 ns;  
4
```

A red arrow points from a blue callout box to the red box. The callout box contains the text: "Dupli klik na ucf fajl otvaramo:".

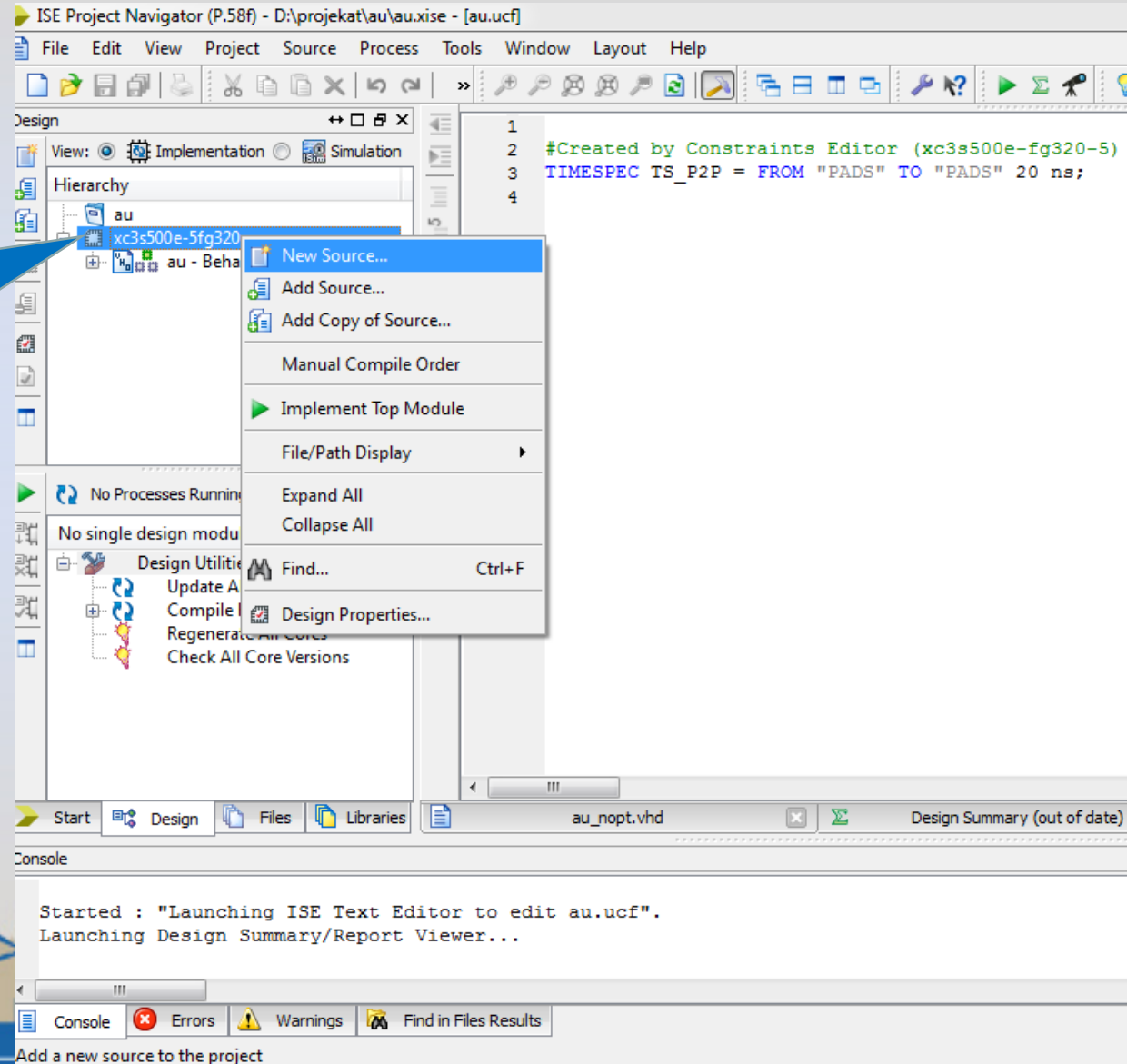
Another blue callout box contains the text: "UCF fajl je tekstualni dokument koji sadrži sva ograničenja, zapisana shodno odgovarajućoj sintaksi, koja su definisana u projektu."

The console window at the bottom shows the following output:

```
Preparing to edit au.ucf...  
Started : "Launching ISE Text Editor to edit au.ucf".
```

Kreiranje novog projektnog fajla - optimizovani kod

Desni klik preko oznake kola, a onda New Source.



The screenshot shows the ISE Project Navigator interface. The 'Hierarchy' view is active, showing a project named 'au' with a sub-project 'xc3s500e-5fg320'. A right-click context menu is open over the 'xc3s500e-5fg320' project, with 'New Source...' selected. The menu options include: 'New Source...', 'Add Source...', 'Add Copy of Source...', 'Manual Compile Order', 'Implement Top Module', 'File/Path Display', 'Expand All', 'Collapse All', 'Find... (Ctrl+F)', and 'Design Properties...'. The 'Design Utilities' section is also visible, containing 'Update All', 'Compile All', 'Regenerate All Cores', and 'Check All Core Versions'. The main editor window shows a VHDL code snippet:

```
1  
2 #Created by Constraints Editor (xc3s500e-fg320-5)  
3 TIMESPEC TS_P2P = FROM "PADS" TO "PADS" 20 ns;  
4
```

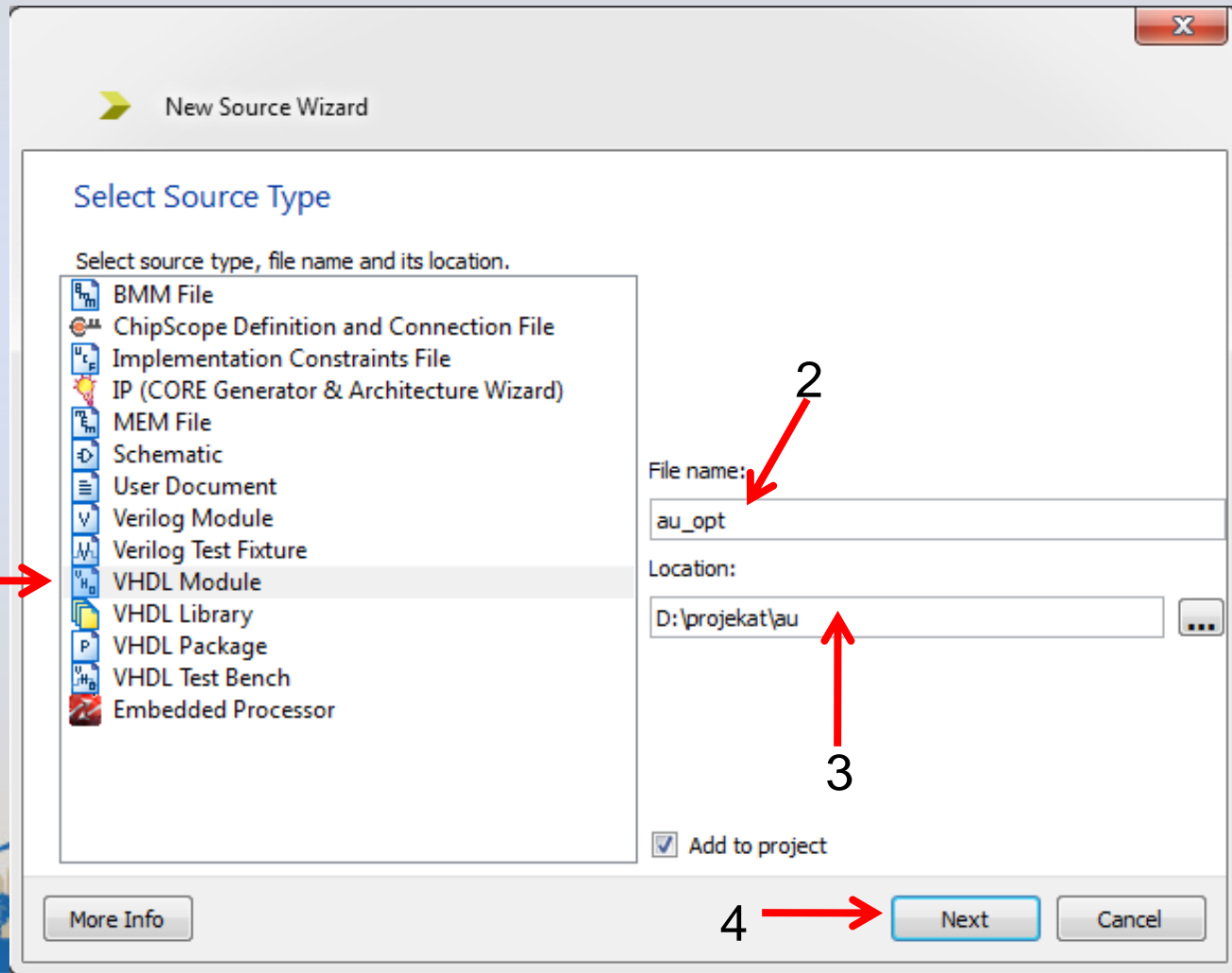
 The console at the bottom displays the message:

```
Started : "Launching ISE Text Editor to edit au.ucf".  
Launching Design Summary/Report Viewer...
```



Kreiranje novog projektnog fajla – optimizovani kod

1. Izbor tipa projektnog fajla (bira se VHDL Module)
2. Upišite ime projektnog fajla (neka bude au_opt)
3. Lokacija - neka ostane predložena lokacija
4. Next



Kreiranje novog projektnog fajla – optimizovani kod

1. Next

New Source Wizard

Define Module

Specify ports for module.

Entity name

Architecture name

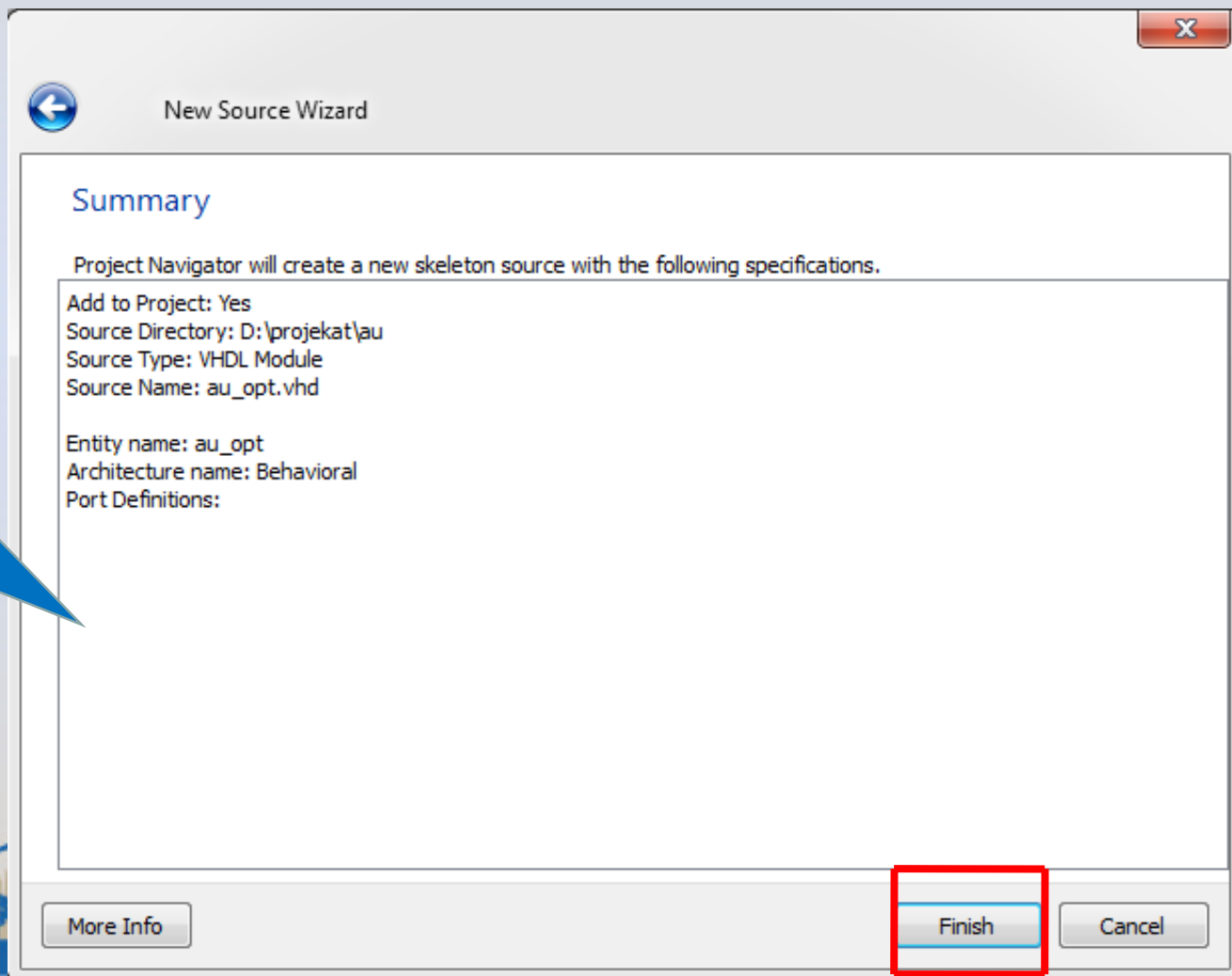
Port Name	Direction	Bus	MSB	LSB
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		

More Info



Kreiranje novog projektnog fajla – optimizovani kod

Informativni dijalog o projektnom fajlu, biramo Finish.



Novi modul – optimizovan kod

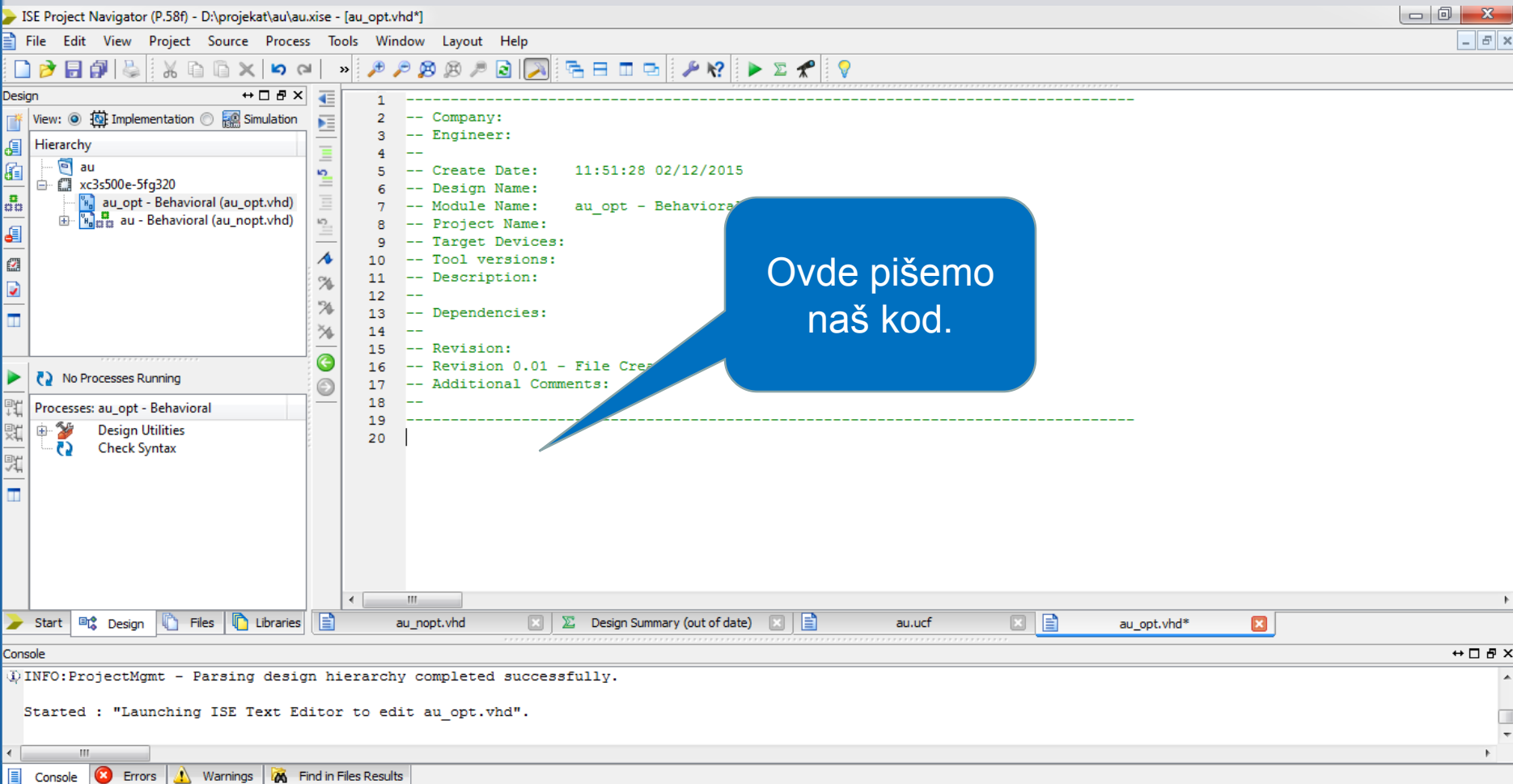
Selektovan je projektni fajl.

The screenshot displays the Xilinx ISE Project Navigator interface. The Design Navigator on the left shows a project hierarchy with 'au_opt - Behavioral (au_opt.vhd)' selected. The main editor window shows the VHDL code for 'au_opt.vhd'. The code includes a header section with metadata and a library declaration for IEEE STD_LOGIC_1164.ALL. The console at the bottom shows the message: 'INFO:ProjectMgmt - Parsing design hierarchy completed successfully. Started : "Launching ISE Text Editor to edit au_opt.vhd".'

```
1  -----
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    11:51:28 02/12/2015
6  -- Design Name:
7  -- Module Name:    au_opt - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
```

Obrišemo sve i pišemo kod iz početka

Pisanje optimizovanog koda



The screenshot displays the ISE Project Navigator interface. The main window shows a VHDL file named `au_opt.vhd` with the following content:

```
1 -----  
2 -- Company:  
3 -- Engineer:  
4 --  
5 -- Create Date:    11:51:28 02/12/2015  
6 -- Design Name:  
7 -- Module Name:    au_opt - Behavioral  
8 -- Project Name:  
9 -- Target Devices:  
10 -- Tool versions:  
11 -- Description:  
12 --  
13 -- Dependencies:  
14 --  
15 -- Revision:  
16 -- Revision 0.01 - File Created  
17 -- Additional Comments:  
18 --  
19 -----  
20
```

A blue callout bubble with white text points to the code area, containing the text: "Ovde pišemo naš kod." (Here we write our code.)

The interface also shows a Hierarchy tree on the left, a Processes panel with "Design Utilities" and "Check Syntax", and a Console window at the bottom with the following output:

```
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.  
  
Started : "Launching ISE Text Editor to edit au_opt.vhd".
```

Optimizovana arhitektura - kod

Prilikom sistezе koda biće usvojena ova vrednost generičnog parametra

```
19 -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.NUMERIC_STD.ALL;
23
24 entity au_opt is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNT0 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNT0 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNT0 0));
29 END au_opt;
30
31 architecture Behavioral OF au_opt IS
32     SIGNAL au, bu : UNSIGNED(N-1 DOWNT0 0);
33     SIGNAL cu : UNSIGNED (0 DOWNT0 0);
34     SIGNAL s : STD_LOGIC_VECTOR(N-1 DOWNT0 0);
35 BEGIN
36     au <= UNSIGNED(a);
37     bu <= UNSIGNED(b) WHEN c = "00" ELSE
38         UNSIGNED(NOT b);
39     cu <= "0" WHEN c = "00" ELSE
40         "1" ;
41     s <= STD_LOGIC_VECTOR(au + bu + cu);
42     Y <= s WHEN (c = "00" OR c = "01") ELSE
43         a WHEN (c = "10" AND s(15) = '1') OR (c = "11" AND s(15) = '0') ELSE
44         b;
45 END Behavioral;
46
```

Pisanje optimizovanog koda

The screenshot displays the ISE Project Navigator (P.58f) interface. The main window shows the VHDL code for a behavioral adder circuit. The code is as follows:

```
19 -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.NUMERIC_STD.ALL;
23
24 entity au_opt is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNTO 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNTO 0));
29 END au_opt;
30
31 architecture Behavioral OF au_opt IS
32     SIGNAL au, bu : UNSIGNED(N-1 DOWNTO 0);
33     SIGNAL cu : UNSIGNED(0 DOWNTO 0);
34     SIGNAL s : STD_LOGIC_VECTOR(N-1 DOWNTO 0);
35 BEGIN
36     au <= UNSIGNED(a);
37     bu <= UNSIGNED(b) WHEN c = "00" ELSE
38         UNSIGNED(NOT b);
39     cu <= "0" WHEN c = "00" ELSE
40         "1";
41     s <= STD_LOGIC_VECTOR(au + bu + cu);
42     Y <= s WHEN (c = "00" OR c = "01") ELSE
43         a WHEN (c = "10" AND s(15) = '1') OR (c = "11" AND s(15) = '0') ELSE
44         b;
45 END Behavioral;
46
```

The interface also shows a Hierarchy view on the left, a Design Utilities panel with options like 'Update All Schematic Files' and 'Compile HDL Simulation Libr...', and a Console window at the bottom with the following output:

```
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit au_opt.vhd".
```

The status bar at the bottom right indicates 'Ln 46 Col 1 VHDL'.

Provera sintakse

Selektovan je projektni fajl.

The screenshot shows the ISE Project Navigator interface. The 'Design' window displays the 'Check Syntax' process as completed. The 'Processes' window shows 'Check Syntax' with a green checkmark. The 'Console' window displays the following output:

```
Entity <au_opt> (Architecture <Behavioral>) compiled.  
Process "Check Syntax" completed successfully
```

The main editor window shows the VHDL code for the 'au_opt' entity, which includes a generic parameter 'N', ports 'a', 'b', 'c', and 'y', and a behavioral architecture.

Dvoklik na Check Syntax.

Poruka da nema sintaksnih grešaka

Implementacija optimizovane arhitekture

Selektovan je projektni fajl.

Dvoklik na Implement Design.

ISE Project Navigator (P.58f) - D:\projekat\au\au.xise - [au_opt.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- au
- xc3s500e-5fg320
- au_opt - Behavioral (au_opt.vhd)
- au - Behavioral (au_nopt.vhd)

```
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.NUMERIC_STD.ALL;
23
24 entity au_opt is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNTO 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNTO 0));
29 END au_opt;
30
31 architecture Behavioral OF au_opt IS
32     SIGNAL au, bu : UNSIGNED(N-1 DOWNTO 0);
33     SIGNAL cu : UNSIGNED (0 DOWNTO 0);
34     SIGNAL s : STD_LOGIC_VECTOR(N-1 DOWNTO 0);
35 BEGIN
36     au <= UNSIGNED(a);
37     bu <= UNSIGNED(b) WHEN c = "00" ELSE
38         UNSIGNED(NOT b);
39     cu <= "0" WHEN c = "00" ELSE
40         "1" ;
41     s <= STD_LOGIC_VECTOR(au + bu + cu);
42     Y <= s WHEN (c = "00" OR c = "01") ELSE
43         a WHEN (c = "10" AND s(15) = '1') OR (c = "11" AND s(15) = '0') ELSE
44         b;
45 END Behavioral;
46
```

Processes Running

- au - Behavioral
- Synthesize - XST
- View RTL Schematic
- View Technology Schematic
- Check Syntax
- Generate Post-Synthesis Si...
- Implement Design**
- Translate
- Map
- Place & Route
- Generate Programming File
- Configure Target Device

Start Design Files Libraries

au_nopt.vhd Design Summary (Implemented) au.ucf

Console

Total time: 1 secs

Process "Generate Post-Place & Route Static Timing" completed successfully

Console Errors Warnings Find in Files Results

Poruka da nema sintaksnih grešaka

Izveštaj o sintezi – neoptimizovan kod

Dvoklik na Design Summary Reports

- Clock Report
- Static Timing
- Errors and Warnings
- Parser Messages
- Synthesis Messages
- Translation Messages
- Map Messages
- Place and Route Messages
- Timing Messages
- Bitgen Messages
- All Implementation Messages
- Detailed Reports
 - Synthesis Report
 - Translation Report
 - Map Report
 - Place and Route Report
 - Post-PAR Static Timing Report
 - Power Report
 - Bitgen Report

- Synthesis Report
 - Top of Report
 - Synthesis Options Summary
 - HDL Compilation
 - Design Hierarchy Analysis
 - HDL Analysis
 - HDL Synthesis
 - HDL Synthesis Report
 - Advanced HDL Synthesis
 - Advanced HDL Synthesis Report

```
# MUXF5 : 16
# VCC : 1
# XORCY : 32
# IO Buffers : 50
# IBUF : 34
# OBUF : 16
```

Device utilization summary:

Selected Device : 3s500efg320-5

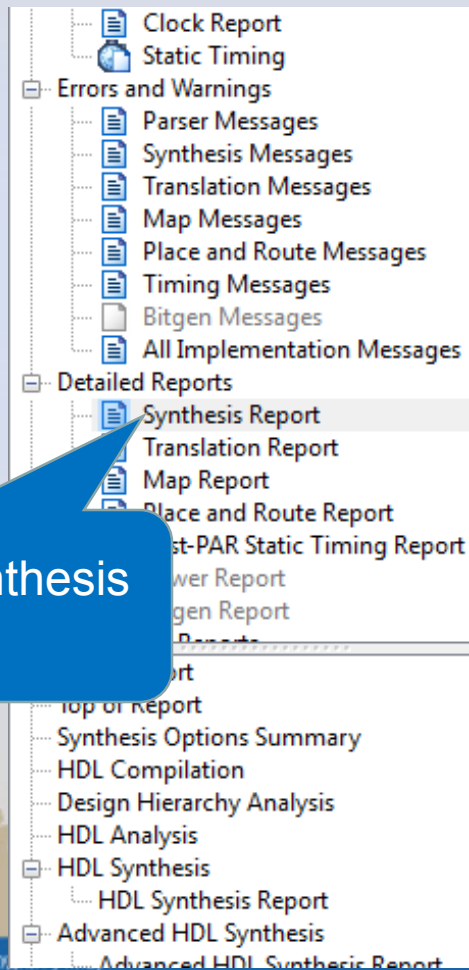
Number of Slices:	49	out of	4656	1%
Number of 4 input LUTs:	97	out of	9312	1%
Number of IOs:	50			
Number of bonded IOBs:	50	out of	232	21%

Partition Resource Summary:

No Partitions were found in this design.

TIMING REPORT

Izveštaj o sintezi – neoptimizovan kod



Upotrebljeni su:
1 16-bitni sabirač,
1 16-bitni oduzimač
1 16-bitni komparator za veće
1 16-bitni komparator za manje
1 16-bitni 4-u-1 multiplekser

Dvoklik na “Synthesis Report”.

```
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors           : 2
 16-bit adder                   : 1
 16-bit subtractor              : 1
# Comparators                   : 2
 16-bit comparator greater      : 1
 16-bit comparator less        : 1
# Multiplexers                  : 1
 16-bit 4-to-1 multiplexer      : 1
```



Izveštaj o sintezi – neoptimizovan kod

Za realizaciju kola u FPGA potreba su 49 slajsa sa iskorišćenih 97 LUT. Broj potrebnih pinova je 50.

The screenshot displays the Synthesis Report interface. The left pane shows a tree view of reports, with 'Synthesis Report' selected under 'Detailed Reports'. The main pane shows the 'Device utilization summary' section, which is highlighted with a red box. Below it, the 'Partition Resource Summary' section is also visible, indicating that no partitions were found in the design.

```
Device utilization summary:
-----
Selected Device : 3s500efg320-5

Number of Slices:                49 out of 4656    1%
Number of 4 input LUTs:          97 out of 9312    1%
Number of IOs:                   50
Number of bonded IOBs:           50 out of 232    21%

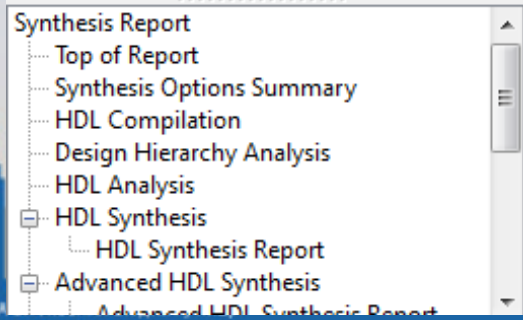
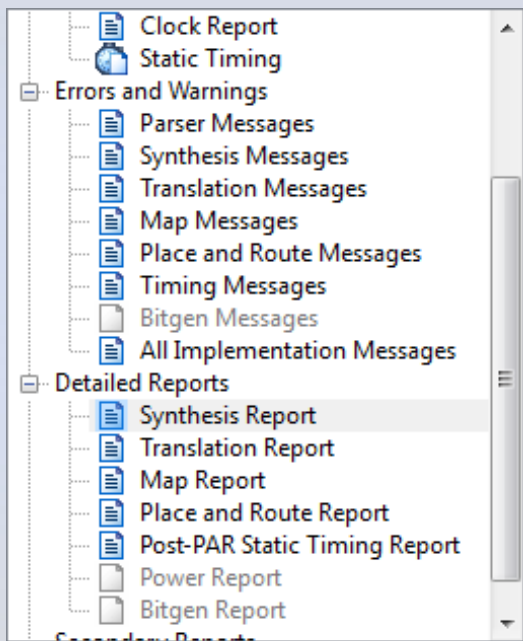
-----
Partition Resource Summary:
-----

No Partitions were found in this design.

-----
TIMING REPORT
```

Izveštaj o sintezi – neoptimizovan kod

Maksimalno propagaciono kašnjenje iznosi 10.417 ns i odgovara kašnjenju signala od ulaza b(0) do izlaza y(15). Na toj putanji se nalazi 22 nivoa logike – 22 redno povezanih LUT-ova).



Timing constraint

Total number of

Delay: 10.417ns (Levels of Logic = 22)
Source: b<0> (PAD)
Destination: y<15> (PAD)

Data Path: b<0> to y<15>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	5	1.106	0.690	b_0_IBUF (b_0_IBUF)
LUT2:I0->O	1	0.612	0.000	Mcompar_max_cmp_gt0000_lut<0> (Mcompar_max_cmp_gt0000_lut<0>)
MUXCY:S->O	1	0.404	0.000	Mcompar_max_cmp_gt0000_cy<0> (Mcompar_max_cmp_gt0000_cy<0>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<1> (Mcompar_max_cmp_gt0000_cy<1>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<2> (Mcompar_max_cmp_gt0000_cy<2>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<3> (Mcompar_max_cmp_gt0000_cy<3>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<4> (Mcompar_max_cmp_gt0000_cy<4>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<5> (Mcompar_max_cmp_gt0000_cy<5>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<6> (Mcompar_max_cmp_gt0000_cy<6>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<7> (Mcompar_max_cmp_gt0000_cy<7>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<8> (Mcompar_max_cmp_gt0000_cy<8>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<9> (Mcompar_max_cmp_gt0000_cy<9>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<10> (Mcompar_max_cmp_gt0000_cy<10>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<11> (Mcompar_max_cmp_gt0000_cy<11>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<12> (Mcompar_max_cmp_gt0000_cy<12>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<13> (Mcompar_max_cmp_gt0000_cy<13>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<14> (Mcompar_max_cmp_gt0000_cy<14>)
MUXCY:CI->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<15> (Mcompar_max_cmp_gt0000_cy<15>)
LUT3:I1->O	1	0.612	0.000	Mcompar_max_cmp_gt0000_lut<1> (Mcompar_max_cmp_gt0000_lut<1>)
LUT3:I0->O	1	0.612	0.000	Mcompar_max_cmp_gt0000_lut<2> (Mcompar_max_cmp_gt0000_lut<2>)
MUXP5:I1->O	1	0.051	0.000	Mcompar_max_cmp_gt0000_cy<16> (Mcompar_max_cmp_gt0000_cy<16>)
OBUF:I->O	3	1.169	0.000	y_9_OBUF (y<9>)

Total 10.417ns (7.914ns logic, 2.504ns route)
(76.0% logic, 24.0% route)

Procena je da kašnjenje kroz logiku (kroz LUT-ove) iznosi 7,914 ns, a kašnjenje kroz veze 2.504 ns).

Izveštaj o implementaciji – neoptimizovan kod

internal clocks in this design. Because there are not defined timing reported in the PAR report in this mode. The PAR timing summary will Note: For the fastest runtime, set the effort level to "std". For b

Device speed data version: "PRODUCTION 1.27 2013-03-26".

Design Summary Report:

Number of External IOBs	50 out of 232	21%
Number of External Input IOBs	34	
Number of External Input IBUFs	34	
Number of External Output IOBs	16	
Number of External Output IOBs	16	
Number of External Bidir IOBs	0	
Number of Slices	49 out of 4656	1%
Number of SLICEMs	0 out of 2328	0%

Overall effort level
Place effort level

Dvoklik na Place and Route Report.

Utrošeno je 49 slajsa.

Izveštaj o implementaciji – neoptimizovan kod

SYSTEM_JITTER to account for the unsupported Discrete Jitter and Phase Error.

Timing constraint: TS_P2P = MAXIMUM_DELAY 20.000 ns;
For more information, see From

2400 paths analyzed, 16 endpoints
0 timing errors detected. (0 errors)
Maximum delay is 12.267ns.

Paths for end point y<9> (P17.I)

Slack (slowest paths): 7.733ns (req - data path)
Source: a<1> (PAD)
Destination: y<9> (PAD)
Requirement: 20.000ns
Data Path Delay: **12.267ns** (Levels of Logic = 12)

Maximum Data Path: a<1> to y<9>

Location	Delay type	Delay (ns)	Physical Resource	Logical Resource(s)
N17.I	Tiopi	1.131	a<1>	a<1>
			a_1_IBUF	a_1_IBUF

Dvoklik na Post-PAR Static Timing Report

Maksimalno kašnjenje u implementiranom kolu iznosi 12.267ns – ograničenje od 20 ns je zadovoljeno.

“Design Summary” – neoptimiozvan kod

Dvoklik Summary.

Number of occupied Slices	49
Number of Slices containing only related logic	49
Number of Slices containing unrelated logic	0
Total Number of 4 input LUTs	97
Number of bonded IOBs	50
Average Fanout of Non-Clock Nets	2.54

Performance Summary

Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)
Routing Results:	All Signals Completely Routed
Timing Constraints:	All Constraints Met

Detailed Reports

Status	Generated
Current	Thu Feb 12 11:56:00 2015
Current	Thu Feb 12 11:56:09 2015
Current	Thu Feb 12 11:56:14 2015
Current	Thu Feb 12 11:56:31 2015
Current	Thu Feb 12 11:56:36 2015

[Post-PAR Static Timing Report](#)

Podatak o maksimalnom propagacionom kašnjenju. Otvaramo levim klikom na “All Constraints Met”.

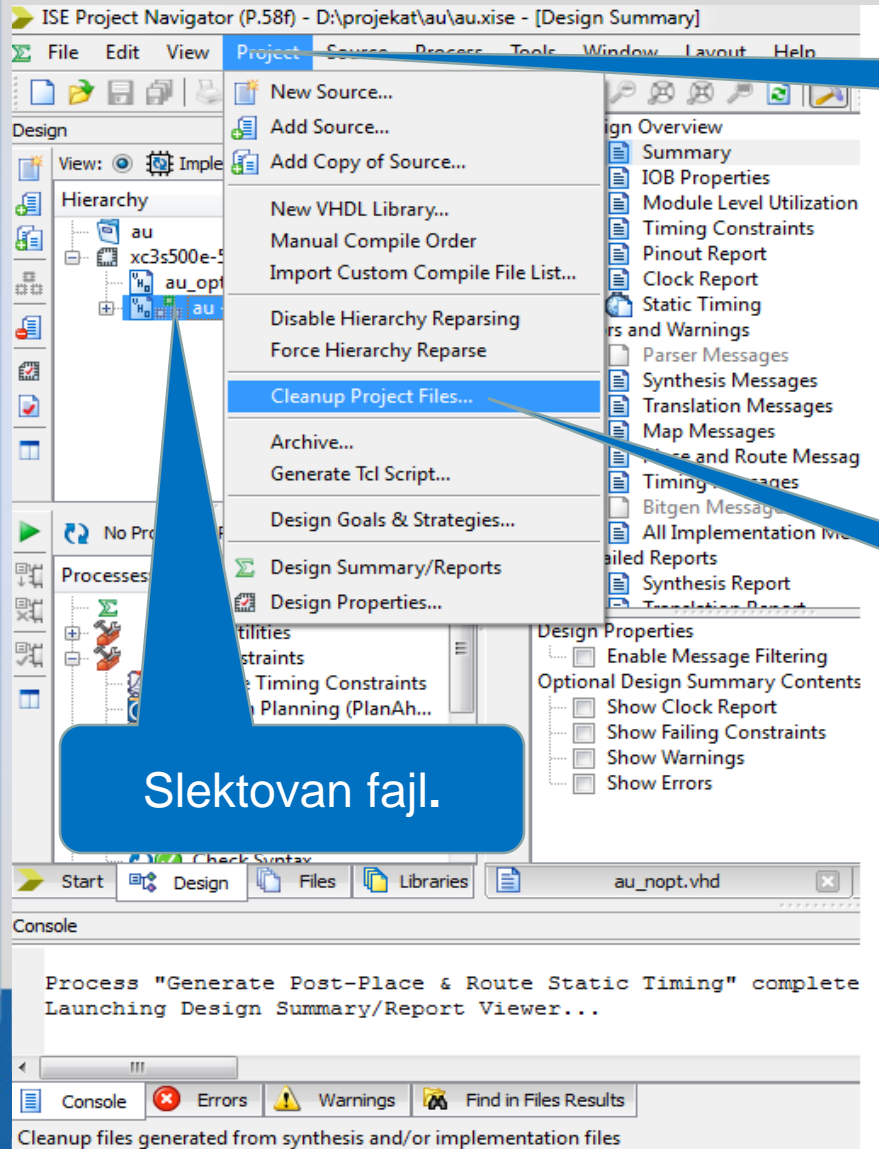
Podatak o maksimalnom propagacionom kašnjenju



The screenshot displays a software interface for timing analysis. On the left, a tree view shows the 'Design Overview' and 'Errors and Warnings' sections. The 'Design Overview' includes Summary, IOB Properties, Module Level Utilization, Timing Constraints (highlighted), Pinout Report, Clock Report, and Static Timing. The 'Errors and Warnings' section includes Parser Messages, Synthesis Messages, Translation Messages, Map Messages, Place and Route Messages, Timing Messages, Bitgen Messages, and All Implementation Messages. Below this is a 'Summary' panel with a 'Show Columns' section where all items (Met, Constraint, Check, Worst Case Slack, Best Case Achievable, Timing Errors, Timing Score) are checked. The main area is a table with the following data:

		Constraint	Check	Worst Case Slack	Best Case Achievable	Timing Errors	Timing Score
1	Yes	TS_P2P = MAXDELAY FROM TIMEGRP "PADS" TO TIMEGRP "PA...	MAXDE...	7.733ns	12.267ns	0	0

“Čišćenje” projektnog fajla – neoptimizovan kod

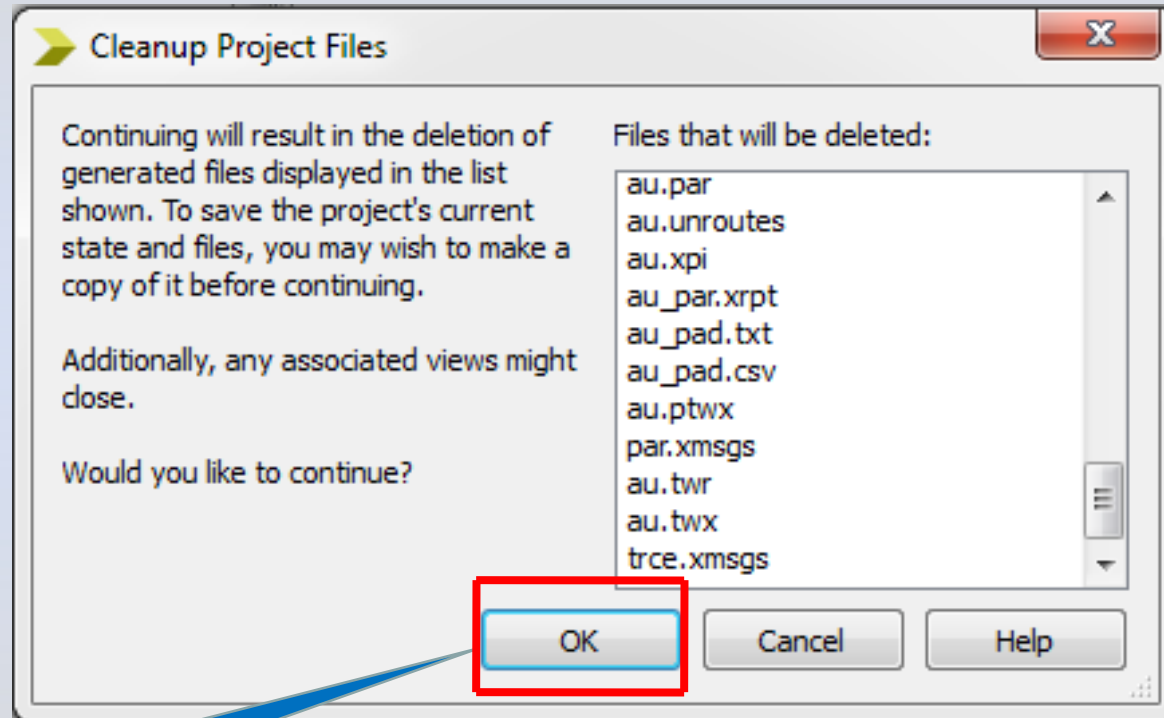


Biramo karticu “Project”.

Slektovan fajl.

Obrisati Projektni fajl
(Cleanup Project Files).

“Čišćenje” projektnog fajla – neoptimizovan kod



Biramo OK.

Prelazak na optimizovanu arhitekturu

Selektovan je projektni fajl. Desnim klikom na slektovani fajl otvaramo novi prozor.

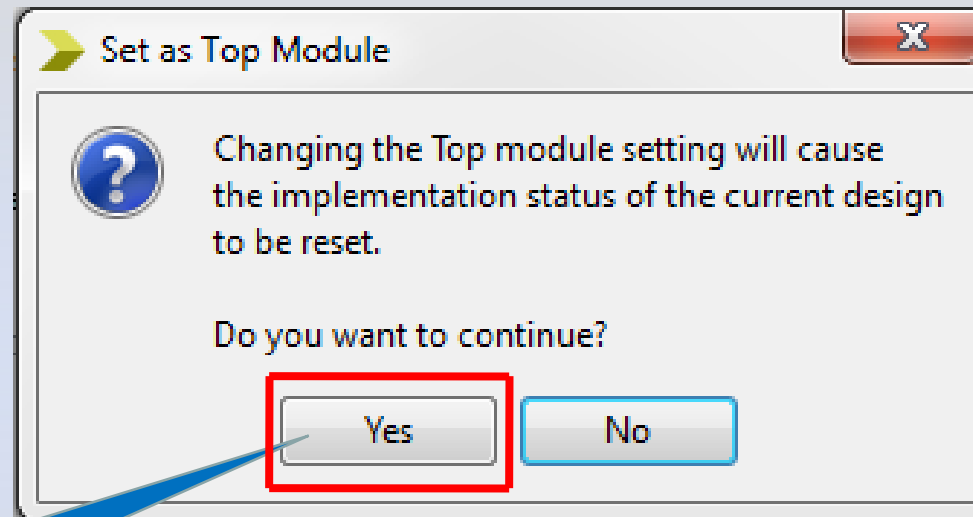
The screenshot shows the ISE Project Navigator interface. The 'Hierarchy' pane on the left shows a project named 'au' with a sub-project 'xc3s500e-5fg320'. A file named 'au_opt - Behavioral (au_opt.vhd)' is selected. A right-click context menu is open over this file, with the 'Set as Top Module' option highlighted. The 'Design Overview' pane on the right shows a list of reports and messages. The 'Console' pane at the bottom shows the following output:

```
Total time: 1 secs  
Process "Generate Post-Place & Route Static Timing" completed successfully
```

At the bottom of the console, a status bar indicates: 'Set the selected module as the top of the design'.

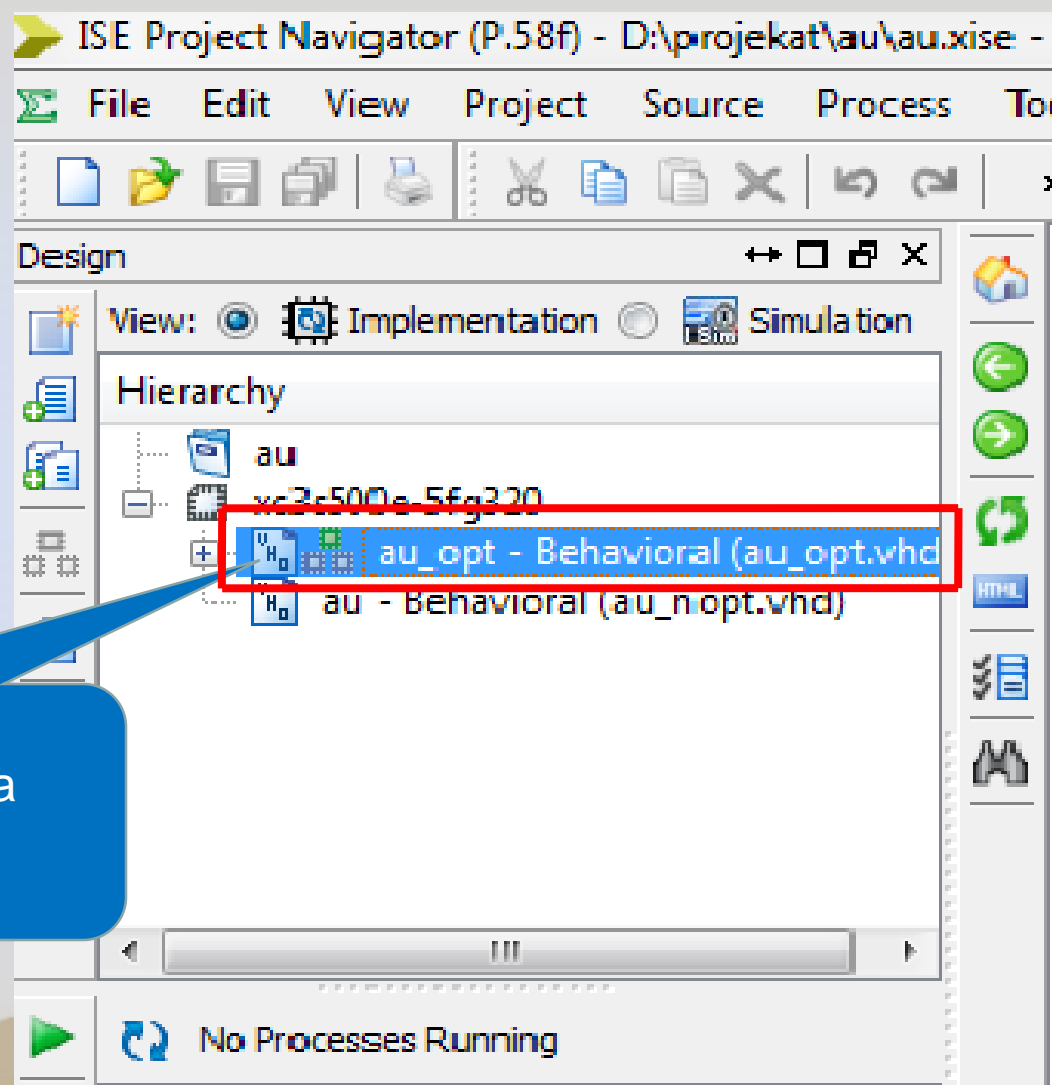
Biramo opciju "Set as Top Module".

Prelazak na optimizovanu arhitekturu



Biramo YES.

Prelazak na optimizovanu arhitekturu



Promenili smo top model na optimizovanu arhitekturu.

Implementacija

Selektovan je projektni fajl.

Dvoklik na Implement Design.

Poruka da je implementacija uspešno okončana.

The screenshot displays the ISE Project Navigator interface for a project named 'au.xise'. The 'Design' window shows a hierarchy with 'au' selected, containing 'xc3s500e-5fg320' and behavioral files. The 'Processes' window shows the 'Implement Design' step completed. The 'Design Overview' window lists various reports, and the 'Console' window shows the successful completion of the implementation process.

ISE Project Navigator (P.58f) - D:\projekat\au\au.xise - [Design Summary (Implemented)]

File Edit View Project Source Process Tools Window Layout Help

Design Overview

- Summary
- IOB Properties
- Module Level Utilization
- Timing Constraints
- Pinout Report
- Clock Report
- Static Timing

Errors and Warnings

- Parser Messages
- Synthesis Messages
- Translation Messages
- Map Messages
- Place and Route Messages
- Timing Messages
- Bitgen Messages
- All Implementation Messages

Detailed Reports

- Synthesis Report
- Translation Report

Design Properties

- Enable Message Filtering

Optional Design Summary Contents

- Show Clock Report
- Show Failing Constraints
- Show Warnings
- Show Errors

Processes: au_opt - Behavioral

- View Technology Schematic
- Check Syntax
- Generate Post-Synthesis Si...
- Implement Design**
- Translate
- Map
- Place & Route
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipSc...

Console

```
Total time: 1 secs  
Process "Generate Post-Place & Route Static Timing" completed successfully
```

Izveštaj o sintezi – optimizovan kod

Dvoklik na Design Summary Reports

- Static Timing
- Errors and Warnings
 - Parser Messages
 - Synthesis Messages
 - Translation Messages
 - Map Messages
 - Place and Route Messages
 - Timing Messages
 - Bitgen Messages
 - All Implementation Messages
- Detailed Reports
 - Synthesis Report
 - Translation Report
 - Map Report
 - Place and Route Report
 - Post-PAR Static Timing Report
 - Power Report
 - Bitgen Report
- Secondary Reports

- Synthesis Report
 - Top of Report
 - Synthesis Options Summary
 - HDL Compilation
 - Design Hierarchy Analysis
 - HDL Analysis
 - HDL Synthesis
 - HDL Synthesis Report
 - Advanced HDL Synthesis
 - Advanced HDL Synthesis Report

```
# XORCY : 16
# IO Buffers : 50
# IBUF : 34
# OBUF : 16
```

Device utilization summary:

Selected Device : 3s500efg320-5

Number of Slices:	25	out of	4656	0%
Number of 4 input LUTs:	34	out of	9312	0%
Number of IOs:	50			
Number of bonded IOBs:	50	out of	232	21%

Partition Resource Summary:

No Partitions were found in this design.

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE

The screenshot shows the Xilinx ISE software interface. On the left, the 'Processes' list is visible, with 'Design Summary/Reports' highlighted. A blue callout bubble points to this option with the text 'Dvoklik na Design Summary Reports'. The main window displays the 'Design Summary' report, which includes the following information:

- Static Timing
- Errors and Warnings
 - Parser Messages
 - Synthesis Messages
 - Translation Messages
 - Map Messages
 - Place and Route Messages
 - Timing Messages
 - Bitgen Messages
 - All Implementation Messages
- Detailed Reports
 - Synthesis Report
 - Translation Report
 - Map Report
 - Place and Route Report
 - Post-PAR Static Timing Report
 - Power Report
 - Bitgen Report
- Secondary Reports

The 'Synthesis Report' section is expanded, showing:

- Top of Report
- Synthesis Options Summary
- HDL Compilation
- Design Hierarchy Analysis
- HDL Analysis
- HDL Synthesis
 - HDL Synthesis Report
 - Advanced HDL Synthesis
 - Advanced HDL Synthesis Report

The 'Device utilization summary' section shows:

```
# XORCY : 16
# IO Buffers : 50
# IBUF : 34
# OBUF : 16
```

The 'Device utilization summary' section shows:

Selected Device : 3s500efg320-5

Number of Slices:	25	out of	4656	0%
Number of 4 input LUTs:	34	out of	9312	0%
Number of IOs:	50			
Number of bonded IOBs:	50	out of	232	21%

The 'Partition Resource Summary' section shows:

No Partitions were found in this design.

The 'TIMING REPORT' section shows:

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE

Izveštaj o sintezi - optimizovan

Dvoklik na
"Synthesis Report".

Static Timing

Errors and Warnings

- Parser Messages
- Synthesis Messages
- Translation Messages
- Map Messages
- Place and Route Messages
- Timing Messages
- Bitgen Messages
- All Implementation Messages

Detailed Reports

- Synthesis Report**
- Translation Report
- Map Report
- Place and Route Report
- PAR Static Timing Report
- Report
- h Report
- ports

Top of Report

- Synthesis Options Summary
- HDL Compilation
- Design Hierarchy Analysis
- HDL Analysis
- HDL Synthesis
 - HDL Synthesis Report
- Advanced HDL Synthesis
 - Advanced HDL Synthesis Report

```
# Adders/Subtractors : 1
16-bit adder carry in : 1

=====
*

Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors : 1
16-bit adder carry in : 1

=====
*
Low Level Synthesis

Optimizing unit <au_opt> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block au_opt, ac
```

Upotrebljeni su:
1 16-bitni sabirač

Izveštaj o sintezi – optimizovan kod

Za realizaciju kola u FPGA potreba su 25 slajsa sa iskorišćenih 34 LUT. Broj potrebnih pinova je 50.

Static Timing

- Errors and Warnings
 - Parser Messages
 - Synthesis Messages
 - Translation Messages
 - Map Messages
 - Place and Route Messages
 - Timing Messages
 - Bitgen Messages
 - All Implementation Messages
- Detailed Reports
 - Synthesis Report
 - Translation Report
 - Map Report
 - Place and Route Report
 - Post-PAR Static Timing Report
 - Power Report
 - Bitgen Report
- Secondary Reports

Synthesis Report

- Top of Report
- Synthesis Options Summary
- HDL Compilation
- Design Hierarchy Analysis
- HDL Analysis
- HDL Synthesis
 - HDL Synthesis Report
 - Advanced HDL Synthesis
 - Advanced HDL Synthesis Report

```
# X
# IO Buf
# I
# O
```

Device utilization summary:

Selected Device : 3s500efg320-5

Number of Slices:	25	out of	4656	0%
Number of 4 input LUTs:	34	out of	9312	0%
Number of IOs:	50			
Number of bonded IOBs:	50	out of	232	21%

Partition Resource Summary:

No Partitions were found in this design.

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE

Izveštaj o implementaciji – optimizovan kod

Static Timing

- Errors and Warnings
 - Parser Messages
 - Synthesis Messages
 - Translation Messages
 - Map Messages
 - Place and Route Messages
 - Timing Messages
 - Bitgen Messages
 - All Implementation Messages
- Detailed Reports
 - Synthesis Report
 - Translation Report
 - Map Report
 - Place and Route Report**
 - Post-PA Static Timing Report
 - Power

Partition Status

Timing Results

Final Summary

```
Initializing temperature to 85.000 Celsius. (default - Range: -40.000 to
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.320 Vol

Device speed data version: "PRODUCTION 1.27 2013-03-26".

Design Summary Report:

Number of External IOBs                50 out of 232    21%
Number of External Input IOBs          34
Number of External Input IBUFs         34
Number of External Output IOBs         1
Number of External Output IOBs        1
Number of External Bidir IOBs

Number of Slices                        25 out of 4656   1%
Number of SLICEMs                       0 out of 2328   0%
```

Dvoklik na Place and Route Report.

Utrošeno je 25 slajsa.

Izveštaj o implementaciji – optimizovan kod

Static Timing

- Errors and Warnings
 - Parser Messages
 - Synthesis Messages
 - Translation Messages
 - Map Messages
 - Place and Route Messages
 - Timing Messages
 - Bitgen Messages
 - All Implementation Messages
- Detailed Reports
 - Synthesis Report
 - Translation Report
 - Map Report
 - Place and Route Report
 - Post-PAR Static Timing Report**
 - Power Report
 - Bitgen Report

SYSTEM_JITTER to account for the unsupported Discrete Jitter and Phase Error.

Timing constraint: TS_P2P = MAX ns;
For more information, see From

1979 paths analyzed, 16 endpoints
0 timing errors detected. (0
Maximum delay is 12.228ns.

Paths for end point y<0> (T17.E

Slack (slowest paths): 7.772ns (requirement - data path)
Source: c<0> (PAD)
Destination: y<0> (PAD)
Requirement: 20.000ns
Data Path Delay: **12.228ns** (Levels of Logic = 12)

Maximum Data Path: c<0> to y<0>

Location	Delay type	Delay(ns)	Physical Resource	Logical Resource(s)
U18.I	Tiopi	1.131	c<0>	c<0>
			c_0_IBUF	c_0_IBUF

Dvoklik na Post-PAR Static Timing Report

Maksimalno kašnjenje u implementiranom kolu iznosi 12.228 ns – ograničenje od 20 ns je zadovoljeno.

Podatak o maksimalnom propagacionom kašnjenju



The screenshot displays a design tool interface with a left-hand navigation pane and a main report area. The navigation pane includes sections for Design Overview, Errors and Warnings, and Detailed Reports. The main report area shows a table of constraints.

	Constraint	Check	Worst Case Slack	Best Case Achievable	Timing Errors	Timing Score	
1	Yes	TS P2P = MAXDELAY FROM TIMEGRP "PADS" TO TIMEGRP "PA...	MAXDE...	5.985ns	14.015ns	0	0

Below the table, a 'Summary' panel is visible, showing a 'Show Columns' section with the following items checked:

- Met
- Constraint
- Check
- Worst Case Slack
- Best Case Achievable
- Timing Errors
- Timing Score



Rezultati sinteze i implementacije neoptimizovane AU

Podaci o implementaciji

RTL komponente

1 sabirač
1 oduzimač
1 komparator za veće
1 komparator za manje
1 multiplexer 4-u-1

Podaci o implementaciji

N (broj bitova)	Slice (broj potrošenih slajsova)	Tp [ns] (max. prop. kašnjenja)
4	11	10.651 ns
8	25	10.298 ns
16	49	12.267 ns

Rezultati sinteze i implementacije optimizovane AU

Podaci o implementaciji

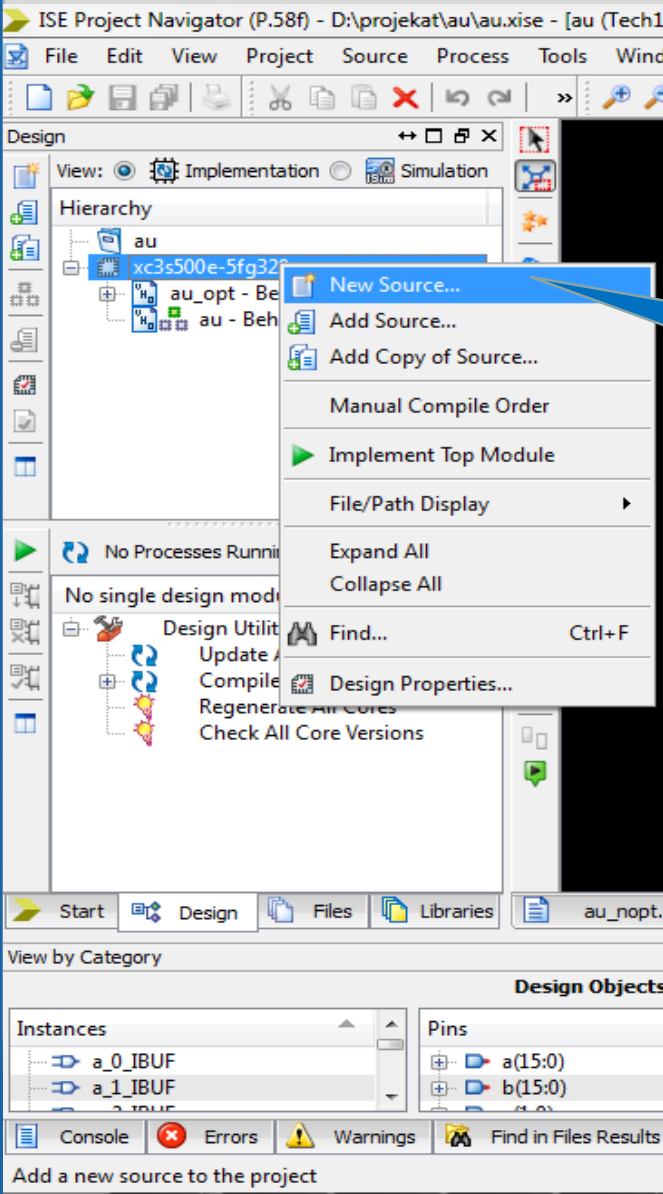
RTL komponente

1 sabirač/oduzimač

Podaci o implementaciji

N (broj bitova)	Slice (broj potrošenih slajsova)	Tp [ns] (max. prop. kašnjenja)
4	7	10.083 ns
8	13	10.759 ns
16	25	12.228 ns

Generisanje testbenča



Desnim klikom preko imena VHDL modula, a onda New Source.

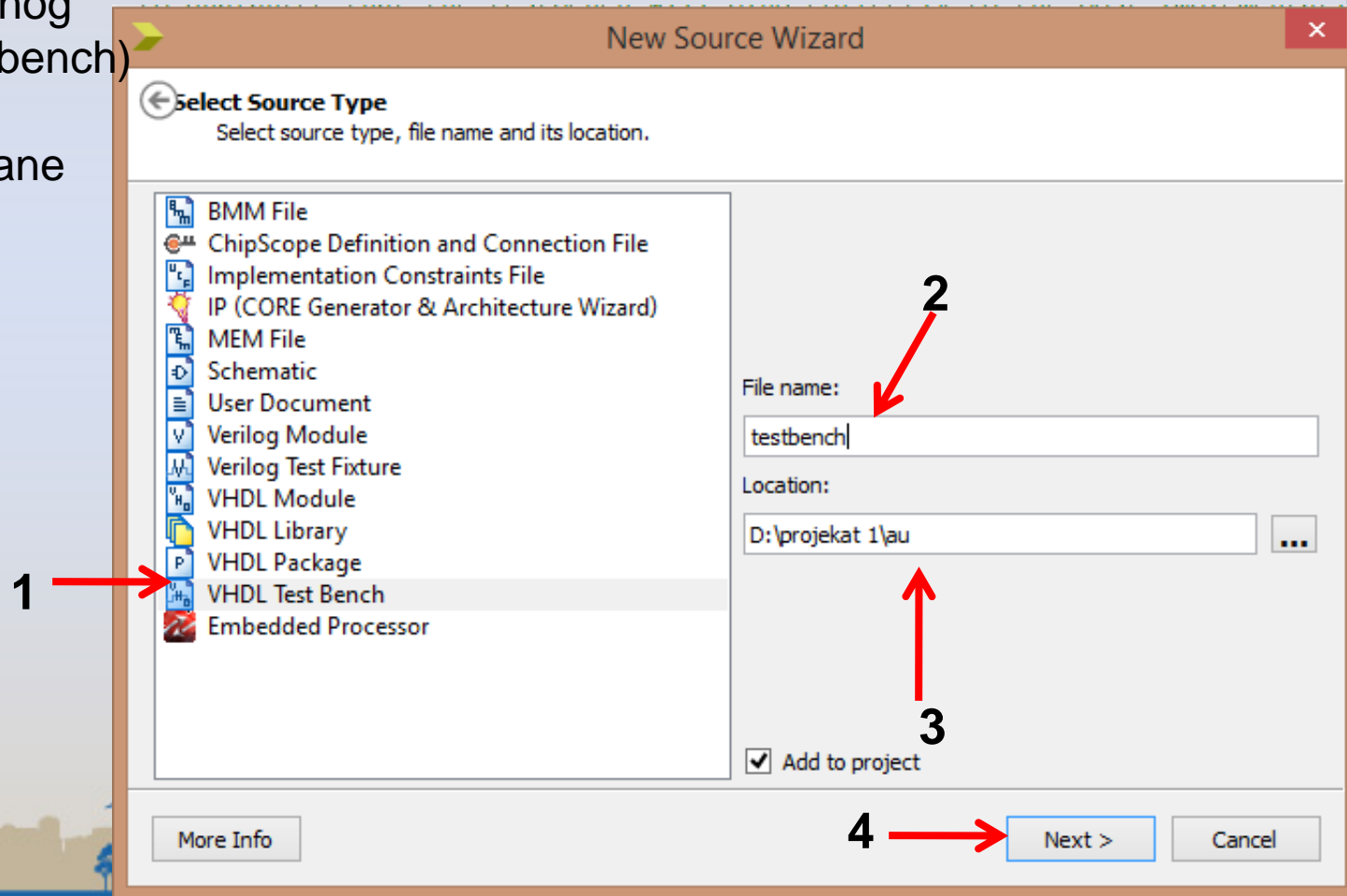
Generisanje testbenča

1. Izbor tipa projektnog fajla
(biraemo VHDL Test Bench)

2. Upišite ime projektnog
fajla (neka bude testbench)

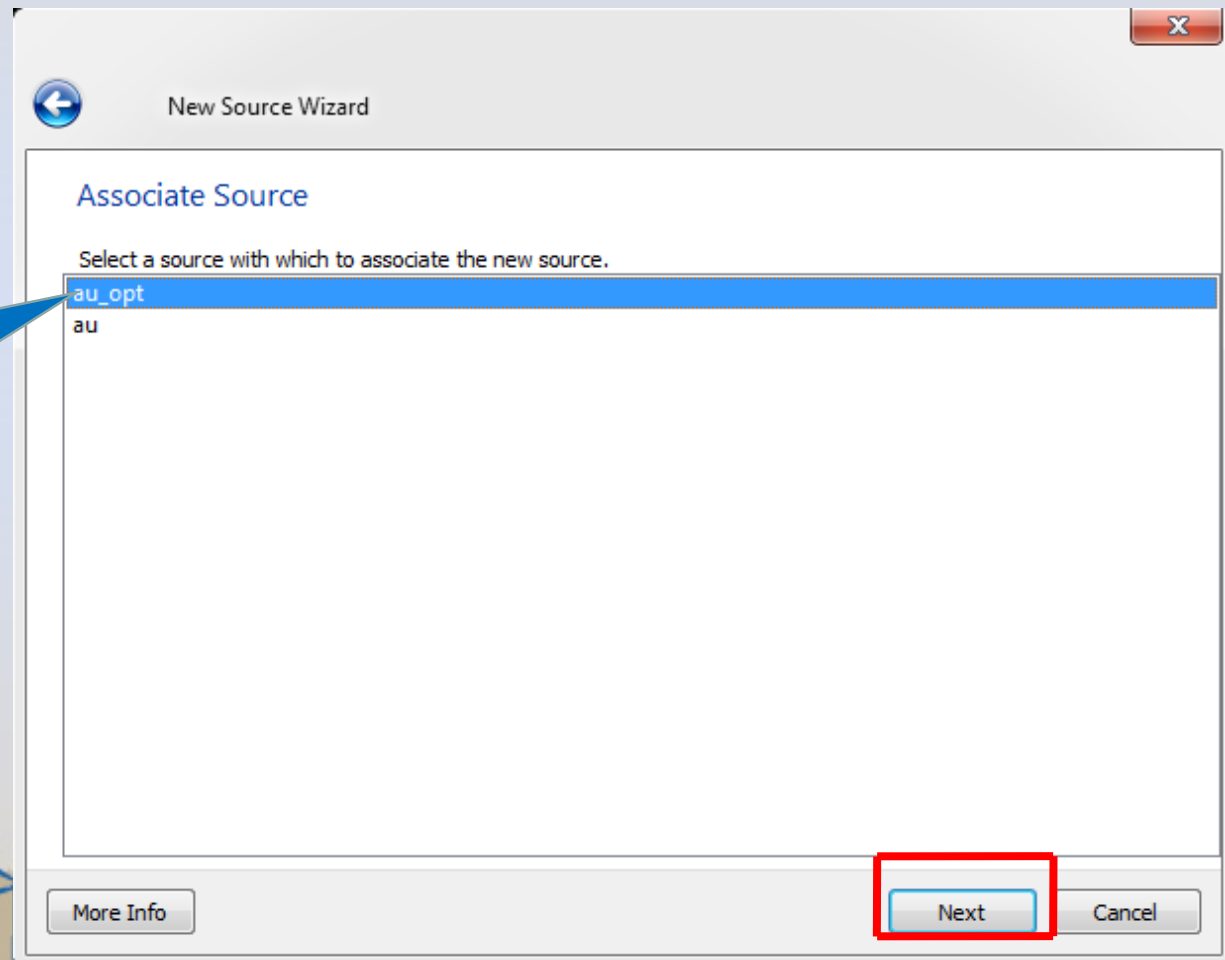
3. Lokacija -neka ostane
predložena lokacija

4. Next



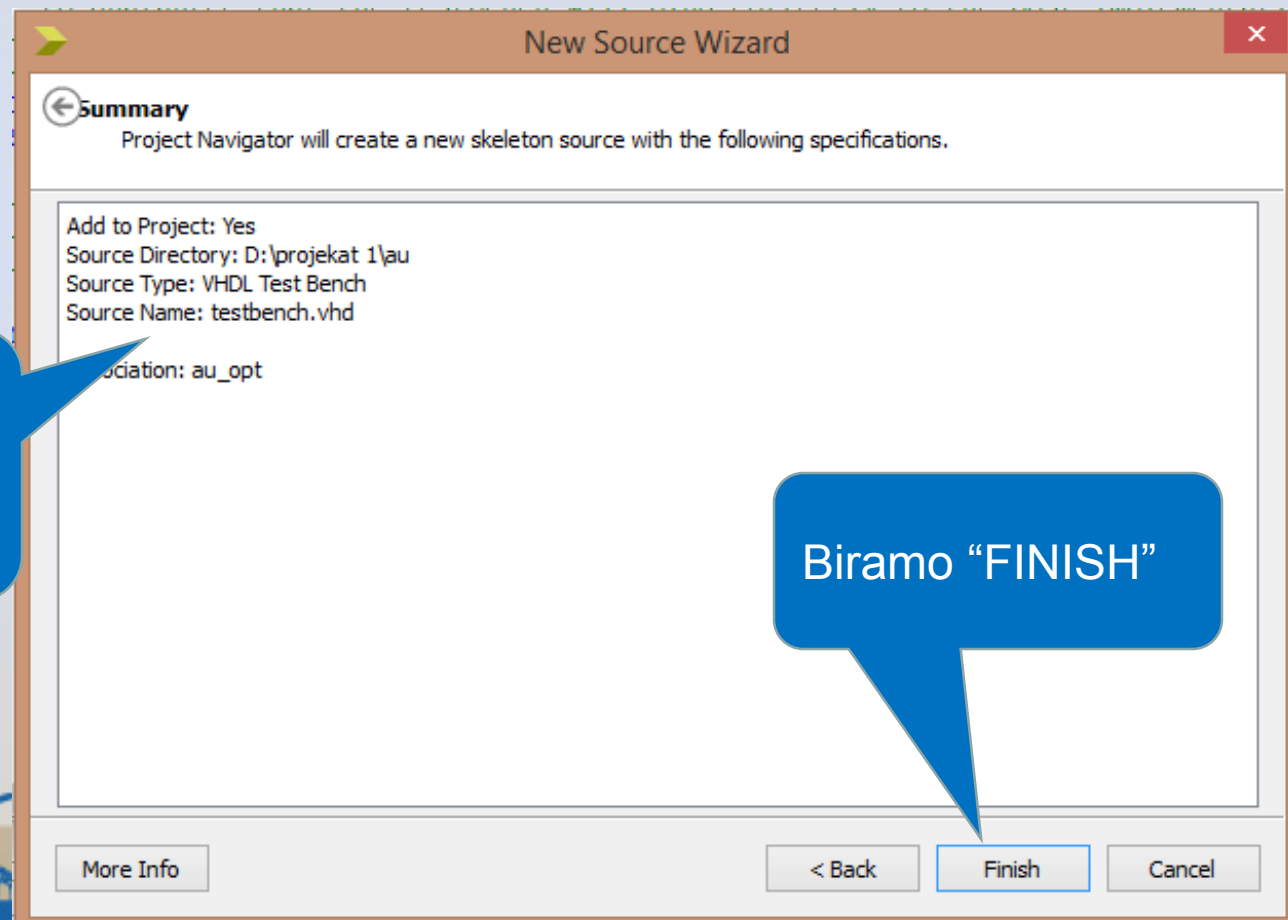
Generisanje testbenča

Mi biramo VHDL Modul "au_opt", pa biramo opciju "Next".



Rezime testbenča

Informativni dijalog o testbenču



Biramo "FINISH"

Testbenč

The screenshot shows the Xilinx ISE Project Navigator interface. The main window displays the VHDL code for a testbench. The left pane shows the project hierarchy with 'au' selected. The bottom pane shows the 'View by Category' section with 'Design Objects of au' and 'Properties of Signal: a_2_IBUF'.

```
5 -- Create Date: 12:36:32 02/12/2015
6 -- Design Name:
7 -- Module Name: D:/projekat/au/au_tb.vhd
8 -- Project Name: au
9 -- Target Device:
10 -- Tool versions:
11 -- Description:
12 --
13 -- VHDL Test Bench Created by ISE for module: au_opt
14 --
15 -- Dependencies:
16 --
17 -- Revision:
18 -- Revision 0.01 - File Created
19 -- Additional Comments:
20 --
21 -- Notes:
22 -- This testbench has been automatically generated using types std_logic and
23 -- std_logic_vector for the ports of the unit under test. Xilinx recommends
24 -- that these types always be used for the top-level I/O of a design in order
25 -- to guarantee that the testbench will bind correctly to the post-implementation
26 -- simulation model.
27 -----
28 LIBRARY ieee;
29 USE ieee.std_logic_1164.ALL;
30
31 -- Uncomment the following library declaration if using
32 -- arithmetic functions with Signed or Unsigned values
```

Ln1 Col1 VHDL

Testbenč

Biramo Simulation.

Biramo testbench – behavior (testbench.vhd).

Obrišemo sve i pišemo kod iz početka

```
LIBRARY ieee;  
USE ieee.std_logic_1164.ALL;  
  
-- Uncomment the following library declaration if using  
-- arithmetic functions with Signed or Unsigned values
```

Testbenč - kod

```
1
2 LIBRARY ieee;
3 USE ieee.std_logic_1164.ALL;
4
5 ENTITY testbench IS
6 END testbench;
7
8 ARCHITECTURE behavior OF testbench IS
9
10     -- Component Declaration for the Unit Under Test (UUT)
11
12     COMPONENT au_opt
13     PORT (
14         a : IN  std_logic_vector(15 downto 0);
15         b : IN  std_logic_vector(15 downto 0);
16         c : IN  std_logic_vector(1 downto 0);
17         y : OUT std_logic_vector(15 downto 0)
18     );
19     END COMPONENT;
20
21
22     --Inputs
23     signal a : std_logic_vector(15 downto 0) := (others => '0');
24     signal b : std_logic_vector(15 downto 0) := (others => '0');
25     signal c : std_logic_vector(1 downto 0) := (others => '0');
26
27     --Outputs
28     signal y : std_logic_vector(15 downto 0);
29     -- No clocks detected in port list. Replace <clock> below with
30     -- appropriate port name
```

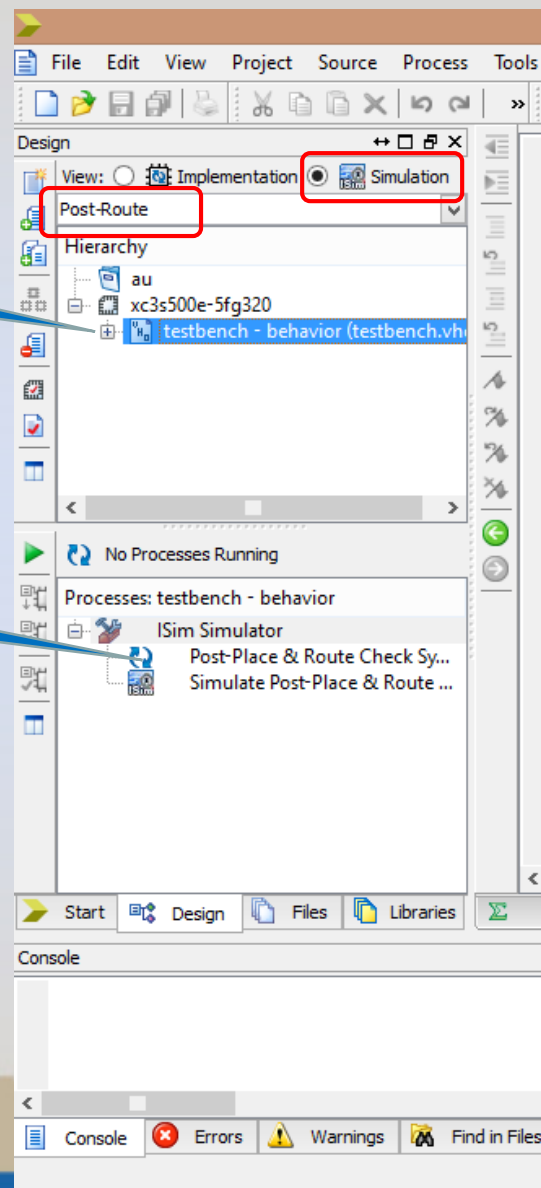
Testbenč - kod

```
35  -- Instantiate the Unit Under Test (UUT)
36  uut: au_opt PORT MAP (
37      a => a,
38      b => b,
39      c => c,
40      y => y
41  );
42
43  -- Stimulus process
44  stim_proc: process
45  begin
46
47      a<="00000000000000001";
48      b<="00000000000001000";
49
50      c<="00";
51      wait for 20 ns;
52
53      a<="00111000000000001";
54      b<="01000000000001100";
55      c<="01";
56      wait for 20 ns;
57      c<="10";
58      wait for 20 ns;
59      c<="11";
60      wait for 20 ns;
61
62  end process;
63
64  END;
```

Provera sintakse i pokretanje simulatora

Selektovanje Testbench-a.

Dvoklik na Post-Place &
Route Check Syntax.



Provera sintakse i pokretanje simulatora

1. Dvoklik na Simulate Behavioral Model.

2. Poruka o ispravnosti sintakse.

The screenshot displays the ISE Project Navigator interface. The 'Design' window shows a hierarchy with 'testbench - behavior (testbench.vhdl)' selected. The 'Processes' window shows 'ISim Simulator' and 'Post-Place & Route Check Syntax' as active processes. The 'Console' window at the bottom shows the message: 'Parsing VHDL file "C:/Users/Stefan/Desktop/projekat/projekat/au/testbench.vhdl"' and 'Process "Post-Place & Route Check Syntax" completed successfully'. The main editor window shows VHDL code for a stimulus process.

```
70     y => y
71   );
72
73
74
75   -- Stimulus process
76   stim_proc: process
77   begin
78
79     a<="000000000000000001";
80     b<="00000000000001000";
81
82     c<="00";
83     wait for 20 ns;
84
85     a<="001110000000000001";
86     b<="01000000000001100";
87     c<="01";
88     wait for 20 ns;
89     c<="10";
90     wait for 20 ns;
91     c<="11";
92     wait for 20 ns;
93
94   end process;
95
96 END;
97
```

Console

```
Parsing VHDL file "C:/Users/Stefan/Desktop/projekat/projekat/au/testbench.vhdl"
Process "Post-Place & Route Check Syntax" completed successfully
```

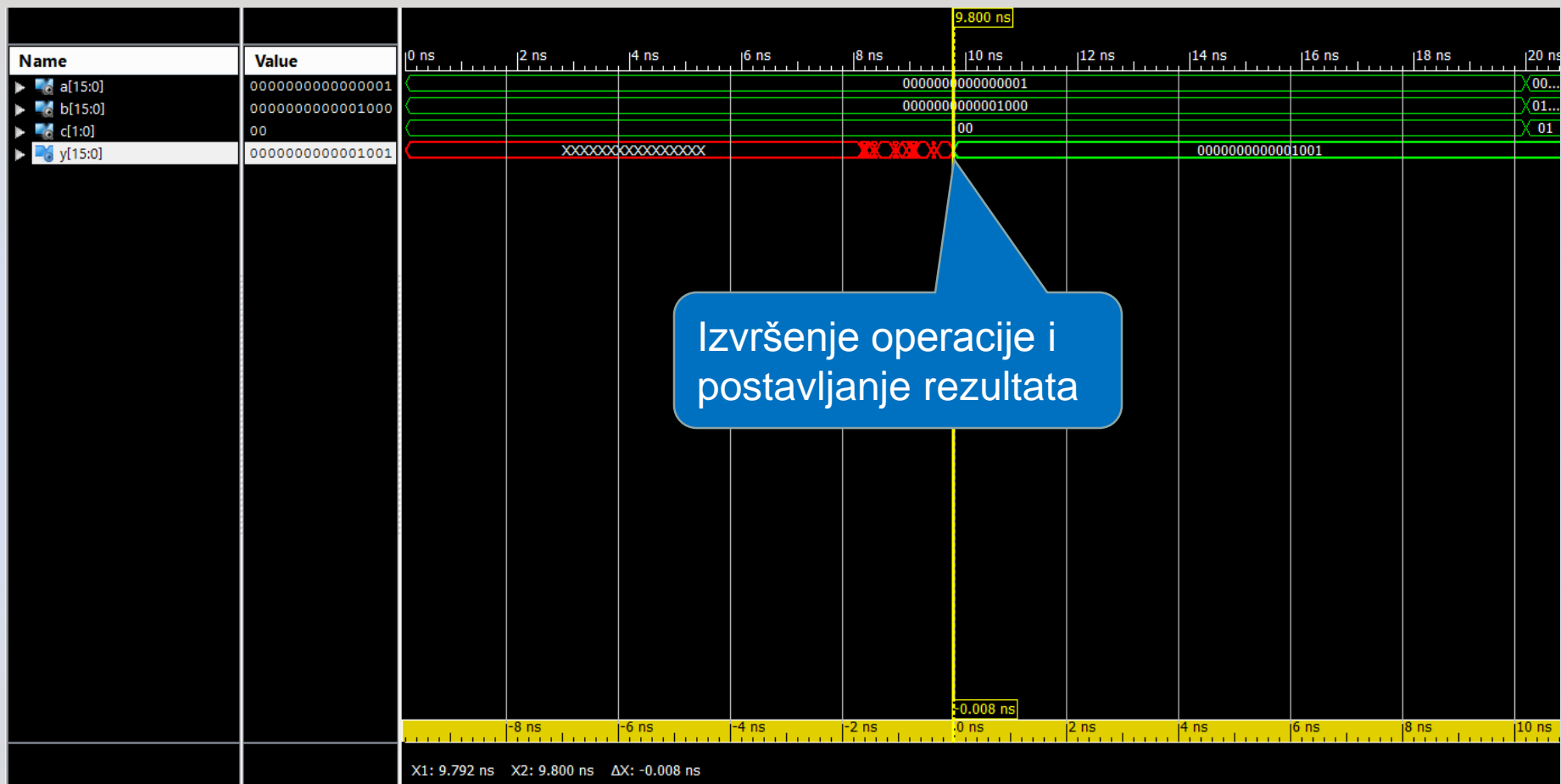
Simulator

1. Zoom

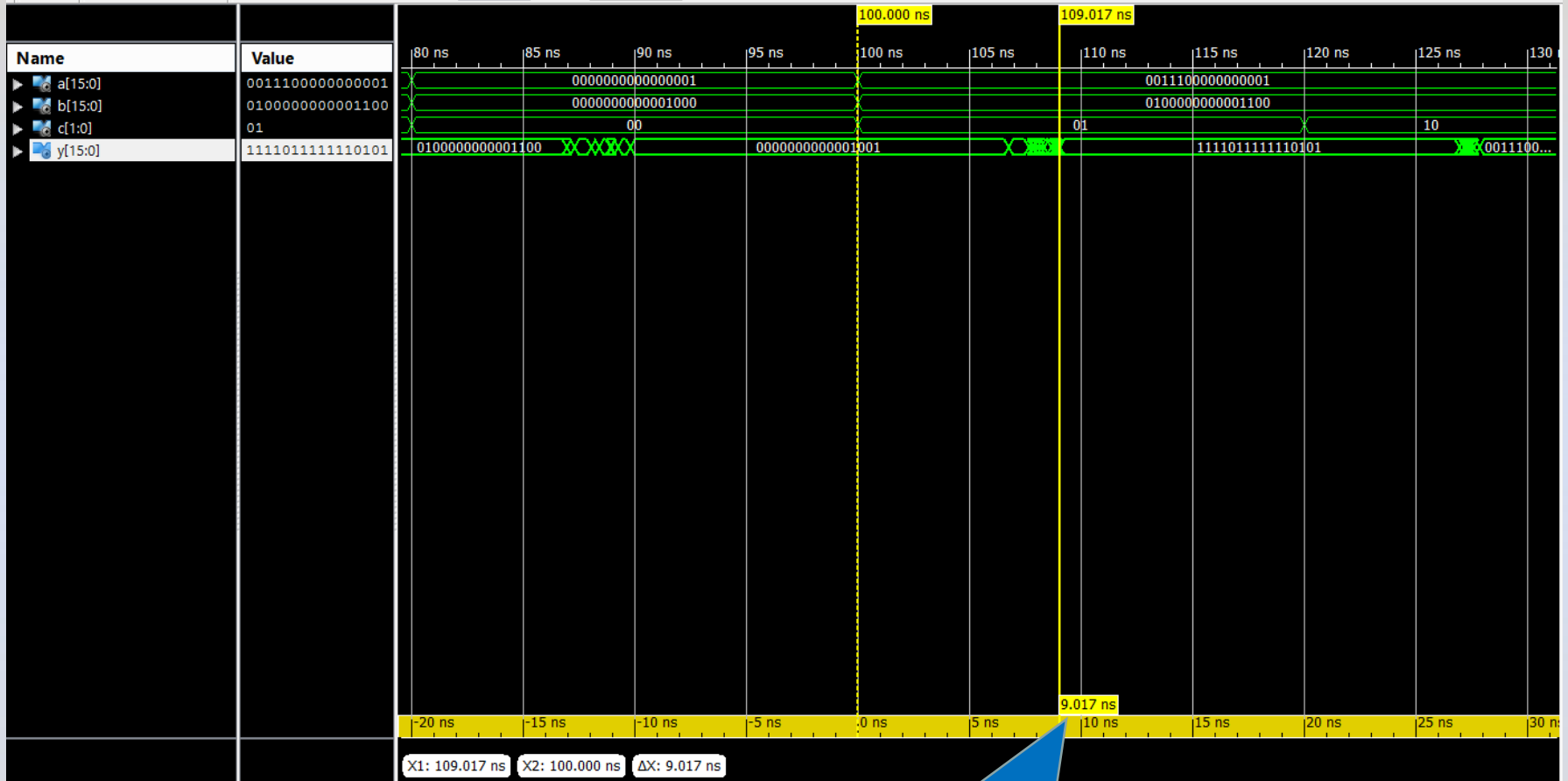
The screenshot shows the ISim (P.58f) - [Default.wcfg] window. The interface includes a toolbar with various simulation controls, a list of variables on the left, and a main display area showing a signal trace. A red box highlights the zoom-in icon in the toolbar. A yellow vertical line is drawn at the 1,000,000 ps mark on the time axis, and the text '1,000,000 ps' is highlighted in yellow above it. The signal trace shows four variables: a[15:0], b[15:0], c[1:0], and y[15:0]. The values are binary strings. The time axis is labeled with values from 999,992 ps to 1,000,001 ps. The status bar at the bottom indicates 'X1: 1,000,000 ps'.

Name	Value	999,992 ps	999,993 ps	999,994 ps	999,995 ps	999,996 ps	999,997 ps	999,998 ps	999,999 ps	1,000,000 ps	1,000,001 ps
a[15:0]	0011100000000001				001110000000001						
b[15:0]	0100000000001100				0100000000001100						
c[1:0]	10				01						
y[15:0]	1111011111110101				1111011111110101						

Simulator

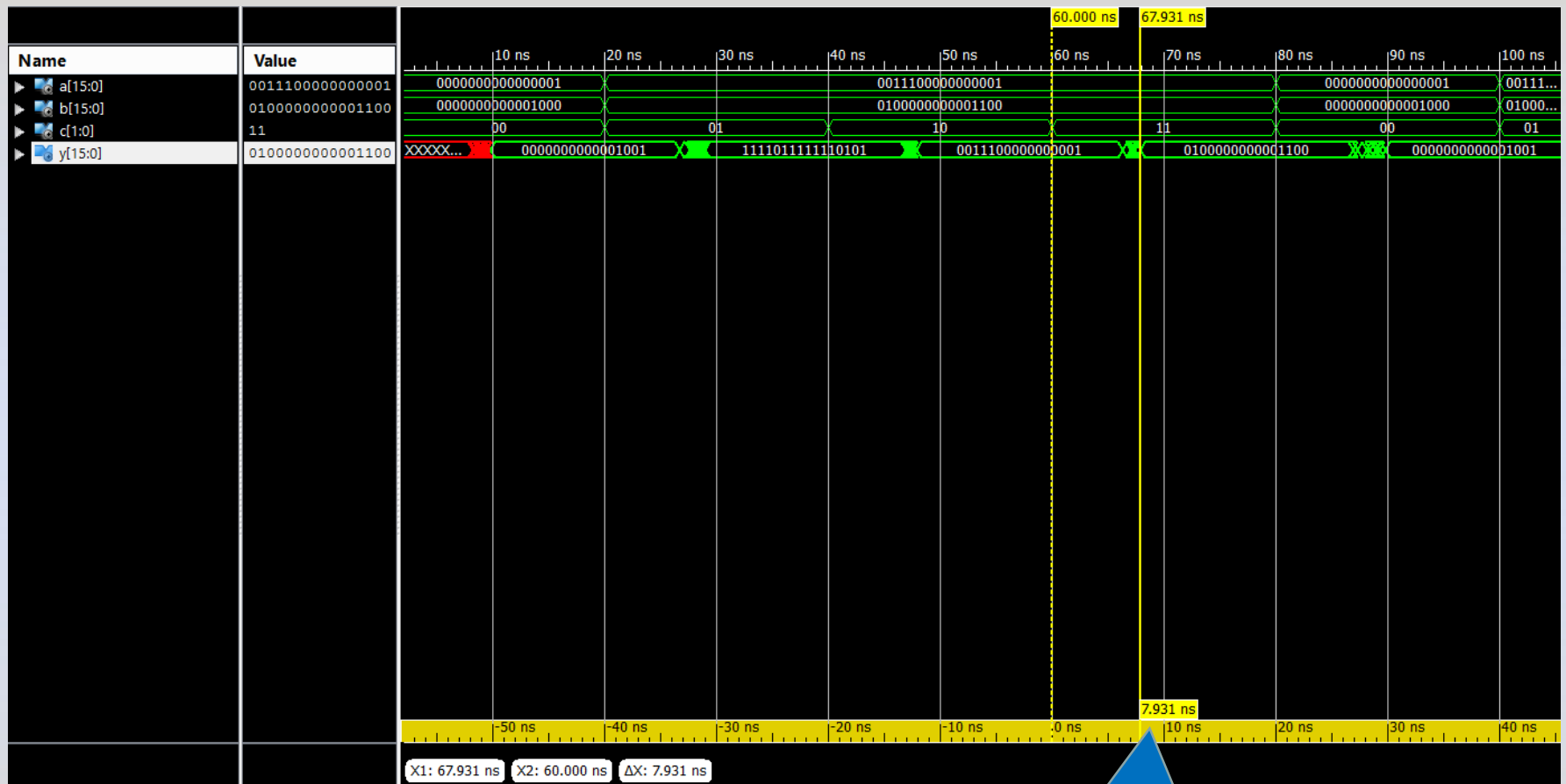


Simulator



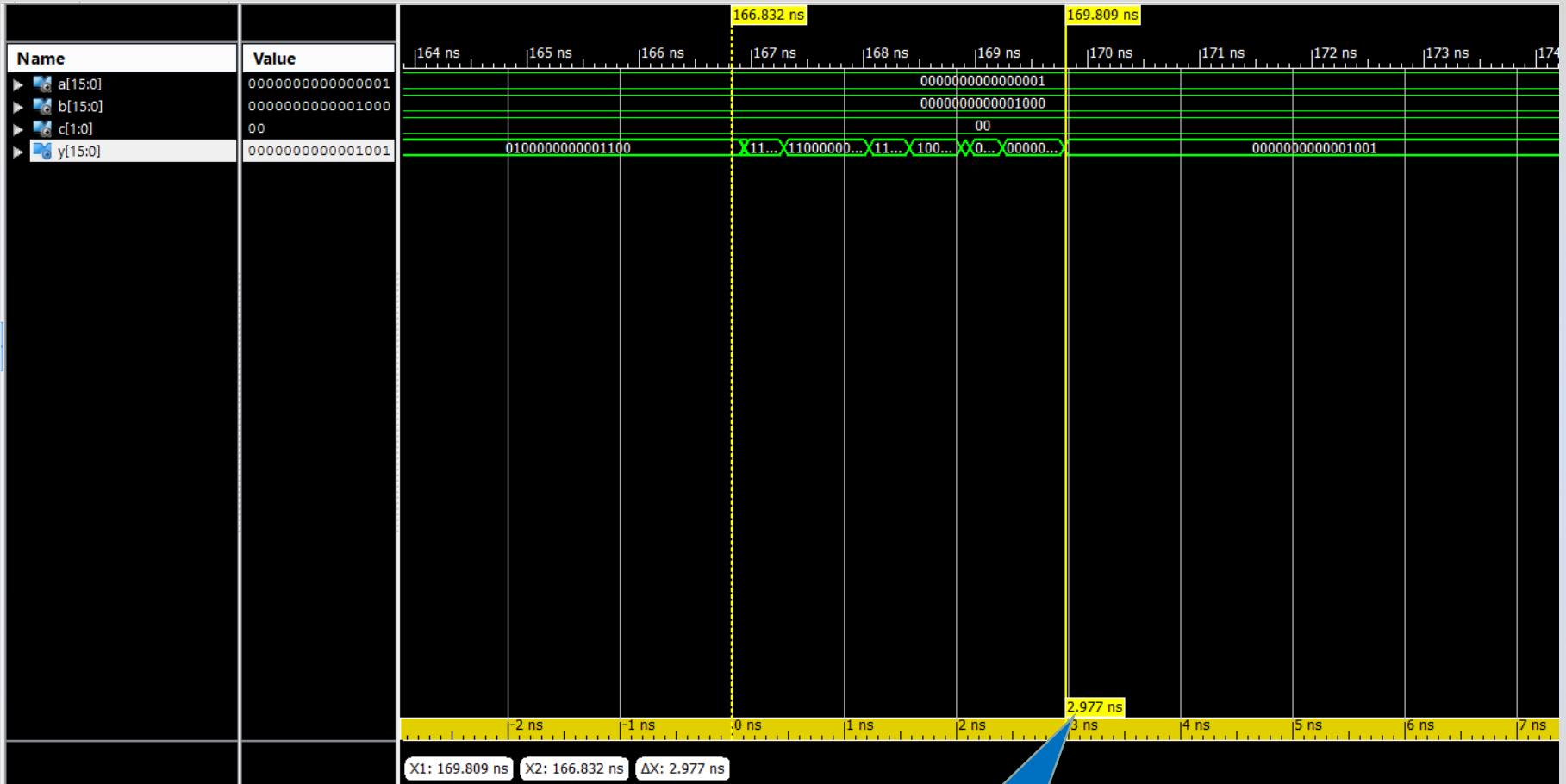
Kašnjenje od trenutka promene jednog od operanada

Simulator



Kašnjenje od trenutka promene tipa operacije

Simulator



Postavljanje rezultata