Projekat iz predmenta Projektovnje pomoću računara - Optimizacija konkurentnog koda

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Studenti:
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Nikolić Stefan SEr 56/13
Đurović Igor REr 19/13

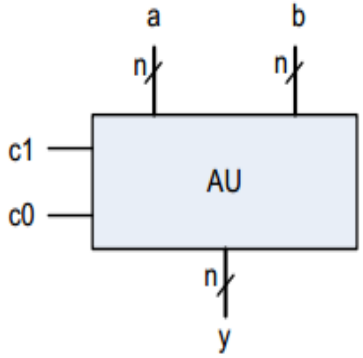
Optimizacija konkurentnog koda

- Cilj: sa što manje hardverskih resursa realizovati željenu funkciju.
- Minimizacija broja aritmetičkih i relacionih operatora u kodu.
- Dve tehnike:

1. Deoba operatora - preurediti kod tako da se se isti operator može iskoristiti za obavljanje više različitih operacija.
2. Deoba funkcija - više funkcija realizuju se tako da dele neke zajedničke delove ili se jedna funkcija koristi za realizaciju neke druge funkcije.

Zadatak

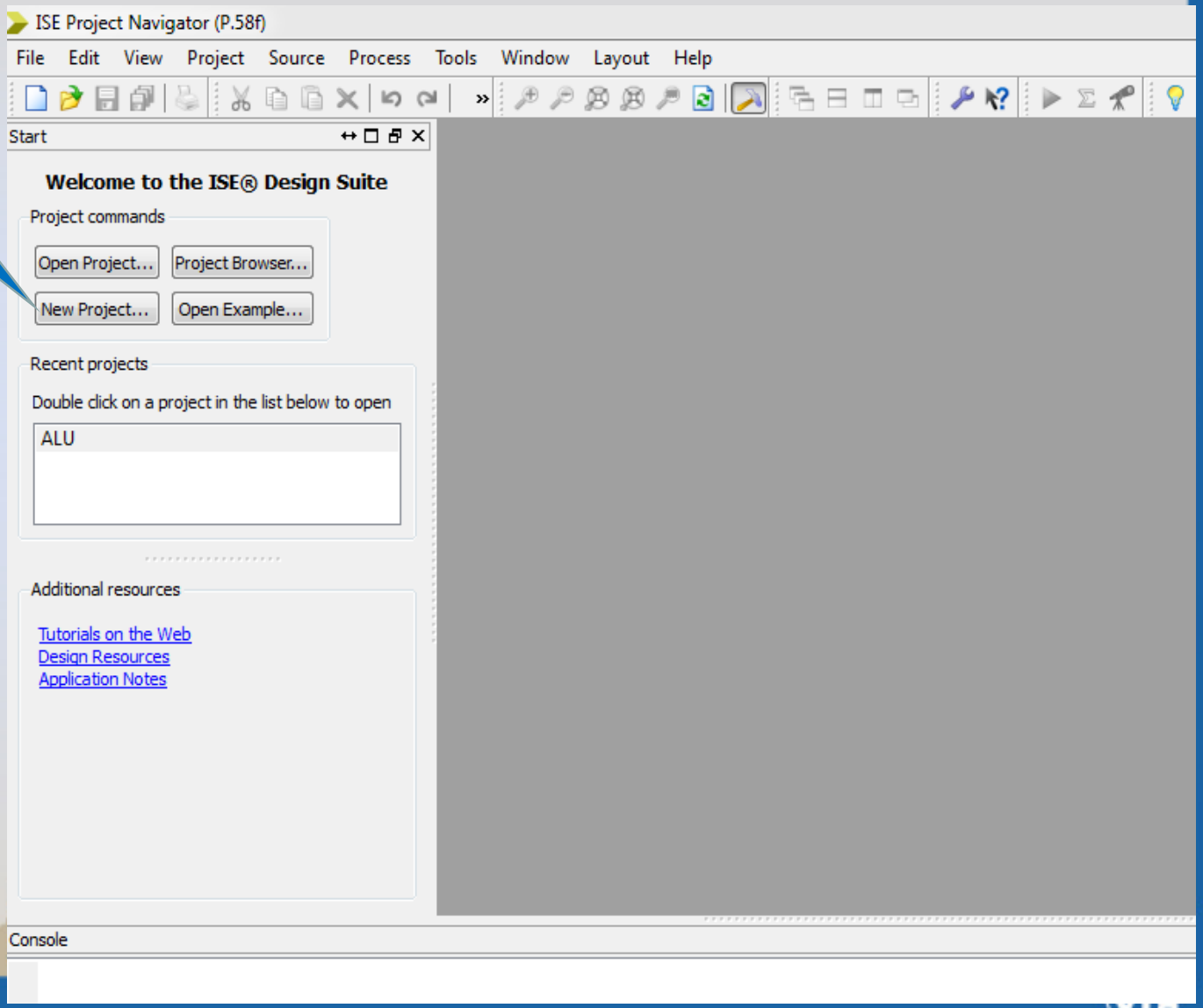
Izvršiti implementaciju dve varijante VHDL opisa višefunkcionalne aritmetičke jedinice na FPGA. Uporediti dva rešenja prema složenosti (zauzeće hardverskih resursa) i performansama (propagaciono kanjenje) za 3 vrednosti gneričkog parametra n: 4, 8 i 16.



c1	c0	Operacija	y
0	0	Sabiranje	a + b
0	1	Oduzimanje	a - b
1	0	Minimum	Min(a, b)
1	1	Maksimum	Max(a, b)

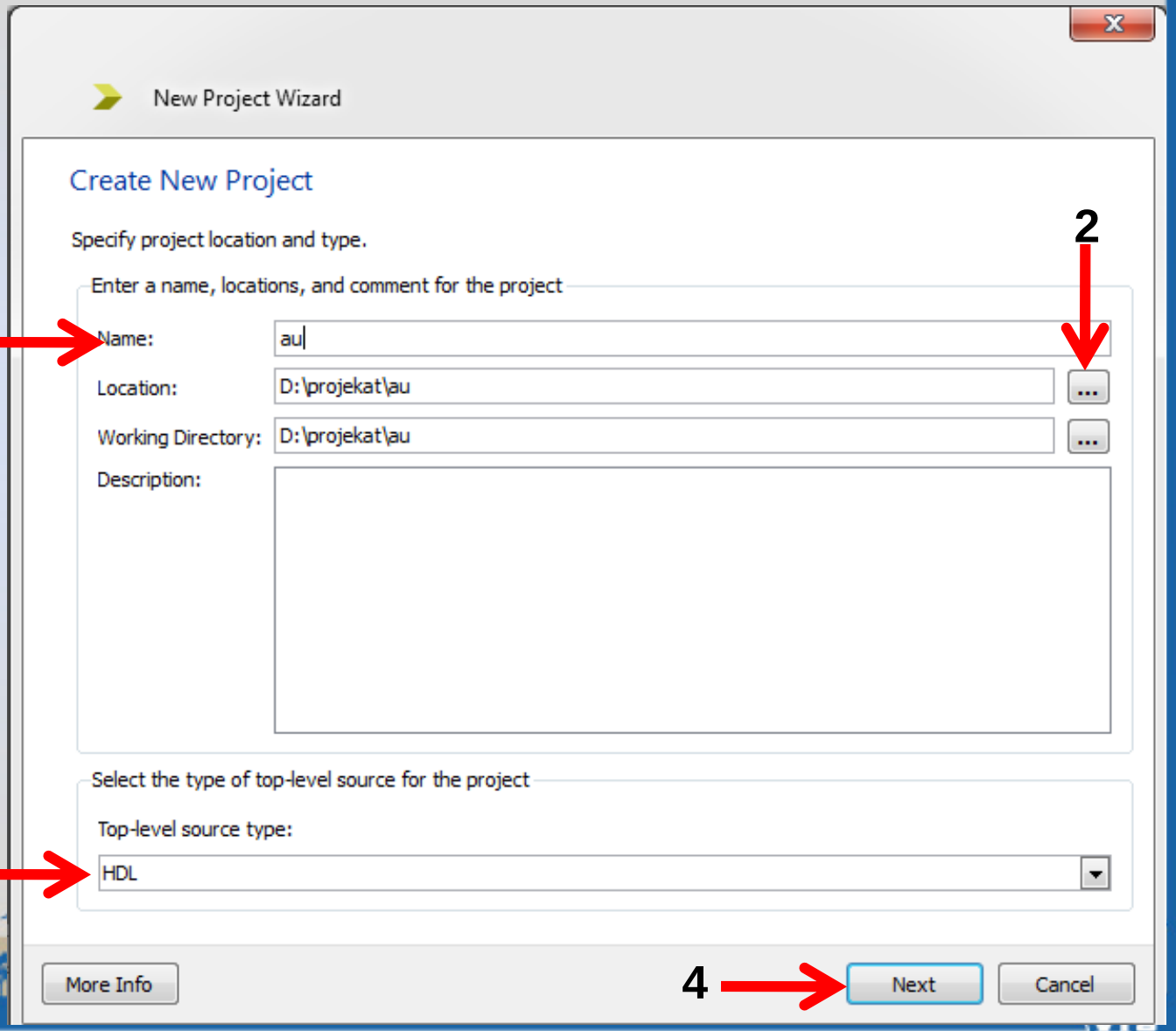
Početak

Biramo New Project za novi projekat.



Kreiranje novog projekta

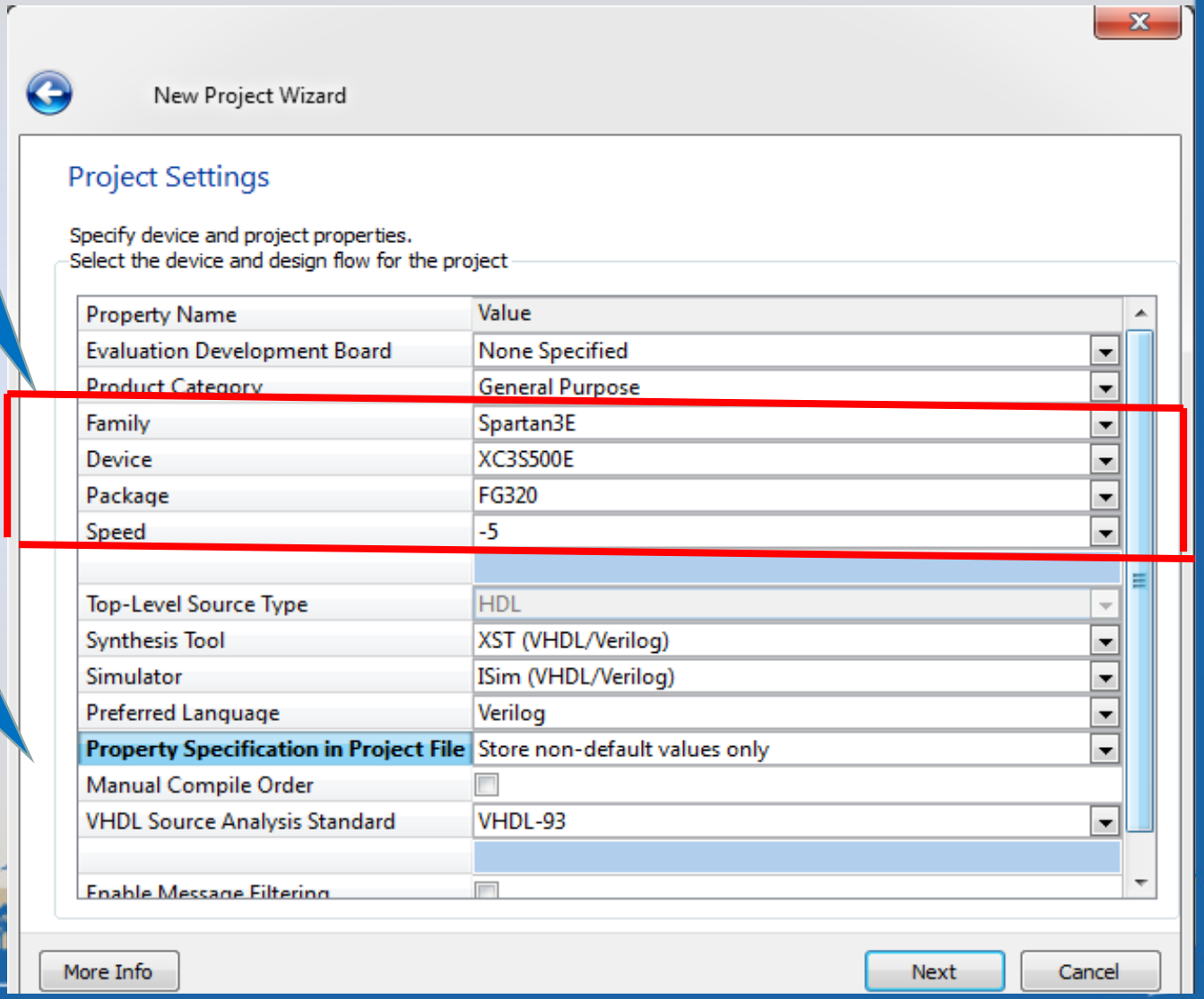
1. Upišite ime projekta.
2. Izaberite lokaciju gde će biti smešten.
3. Izaberite tip projekta. (biramo HDL)
4. NEXT



Izbor integrisanog kola

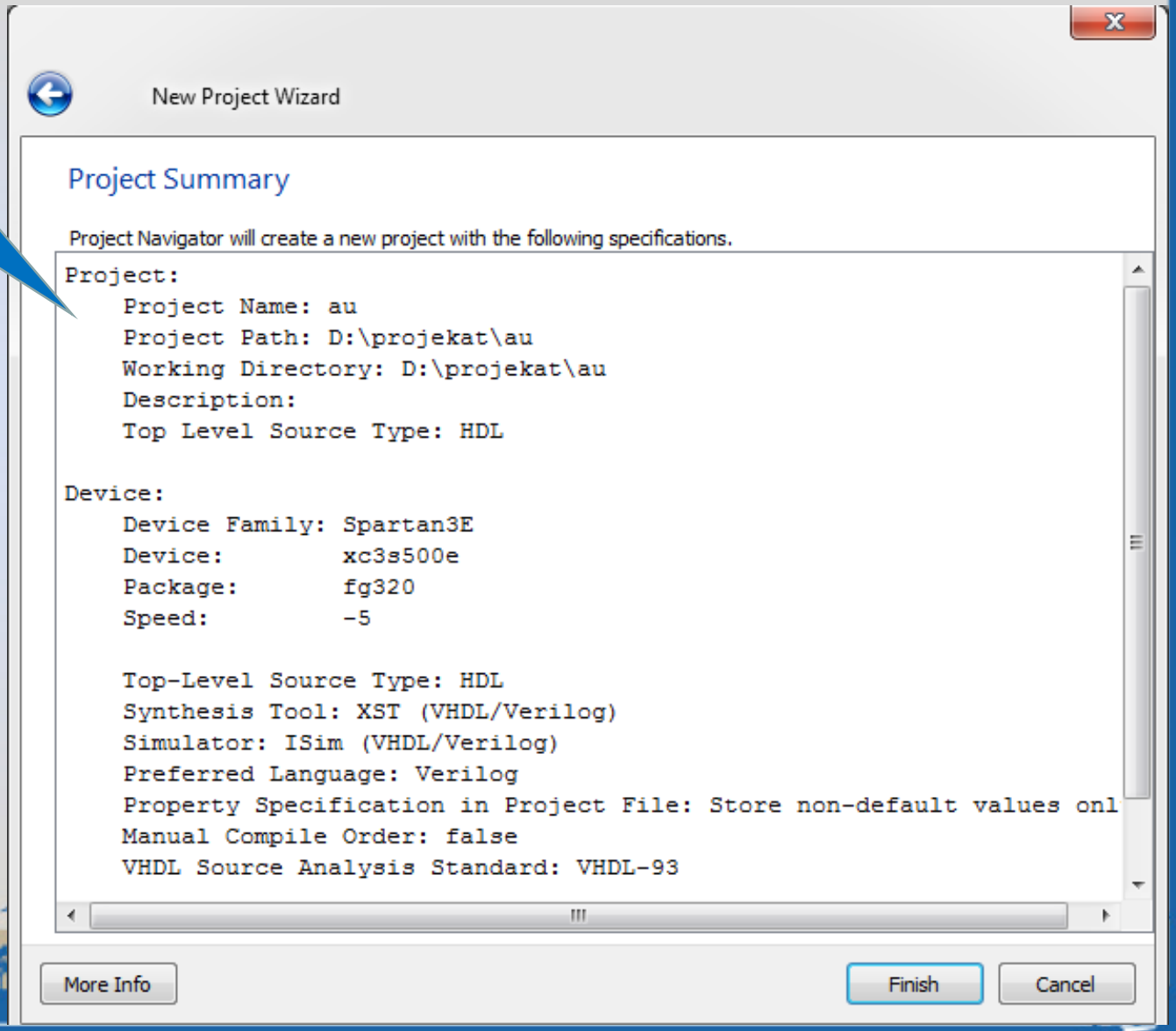
Biramo konkretno kolo za koje će biti realizovan projekat.

Ostalo ostaviti kako jeste, zatim potvrditi sa Next.

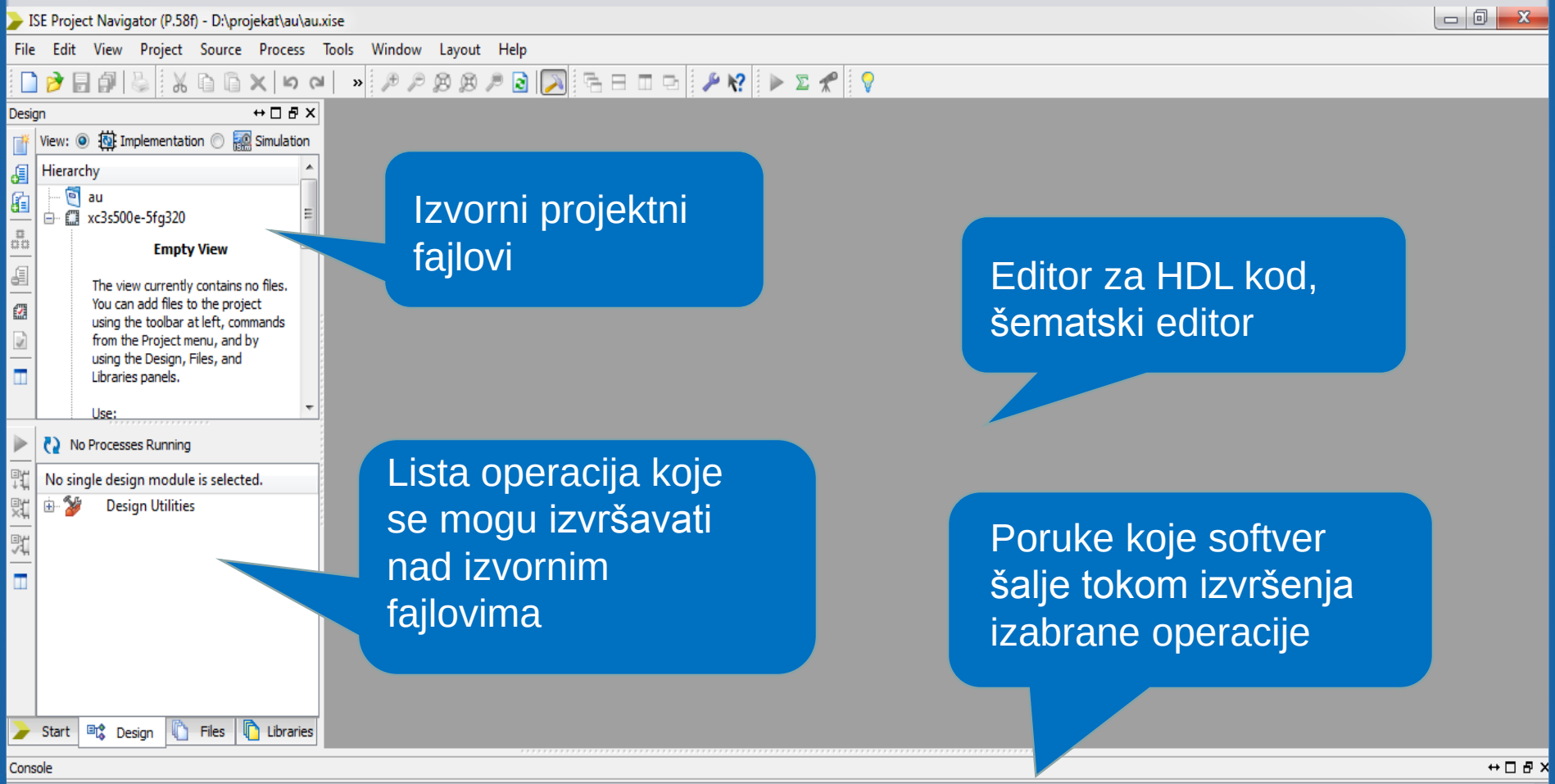


Rezime projekta

Informativni dijalogo projektu, biramo Finish.

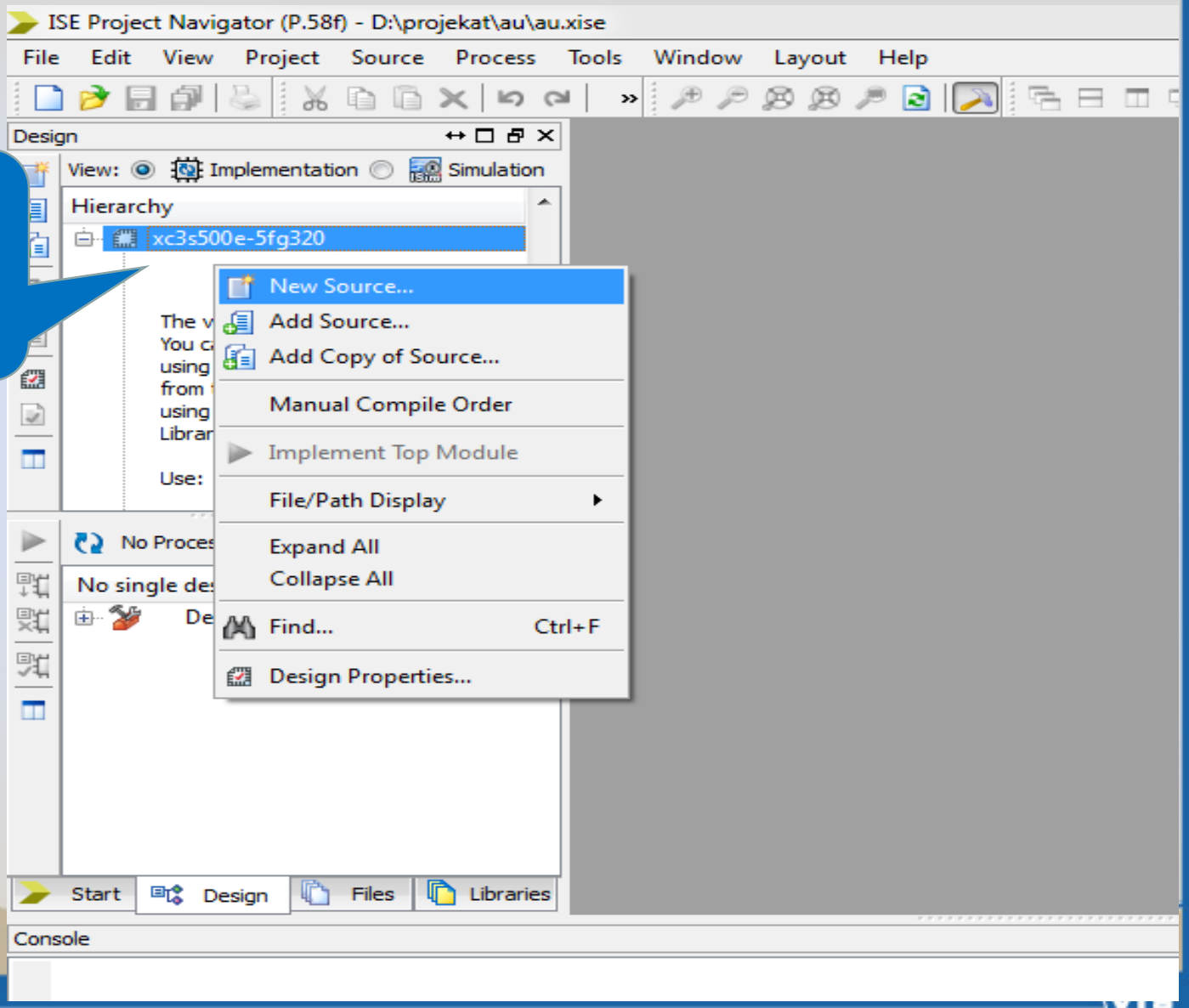


Izgled novog projekta



Kreiranje novog projektnog fajla - neoptimizovan kod

Desni klik preko oznake kola, a onda New Source



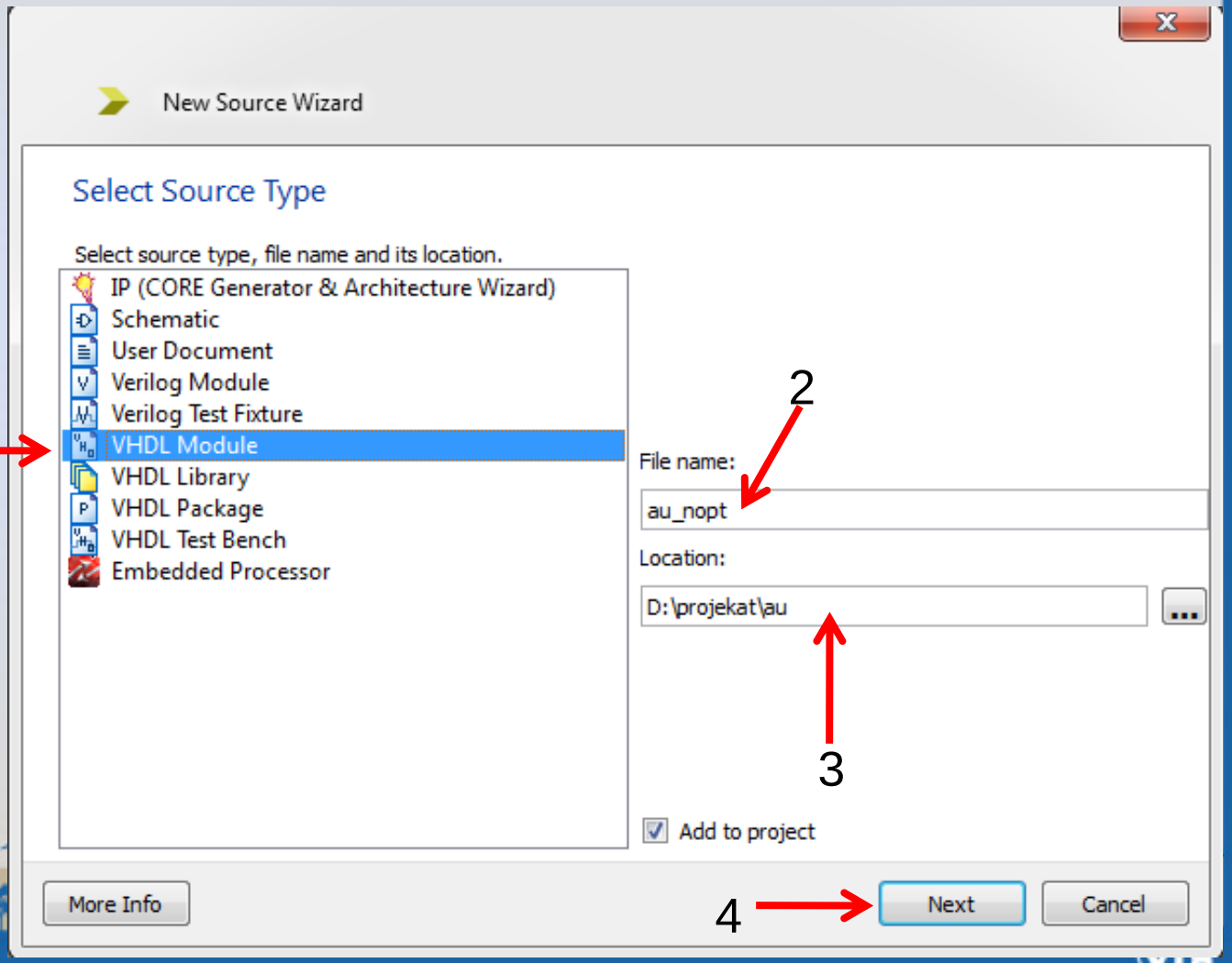
Kreiranje novog projektnog fajla

1.Izbor tipa projektnog fajla (biramoVHDL Module)

2.Upišite ime projektnog fajla (neka bude au_nopt)

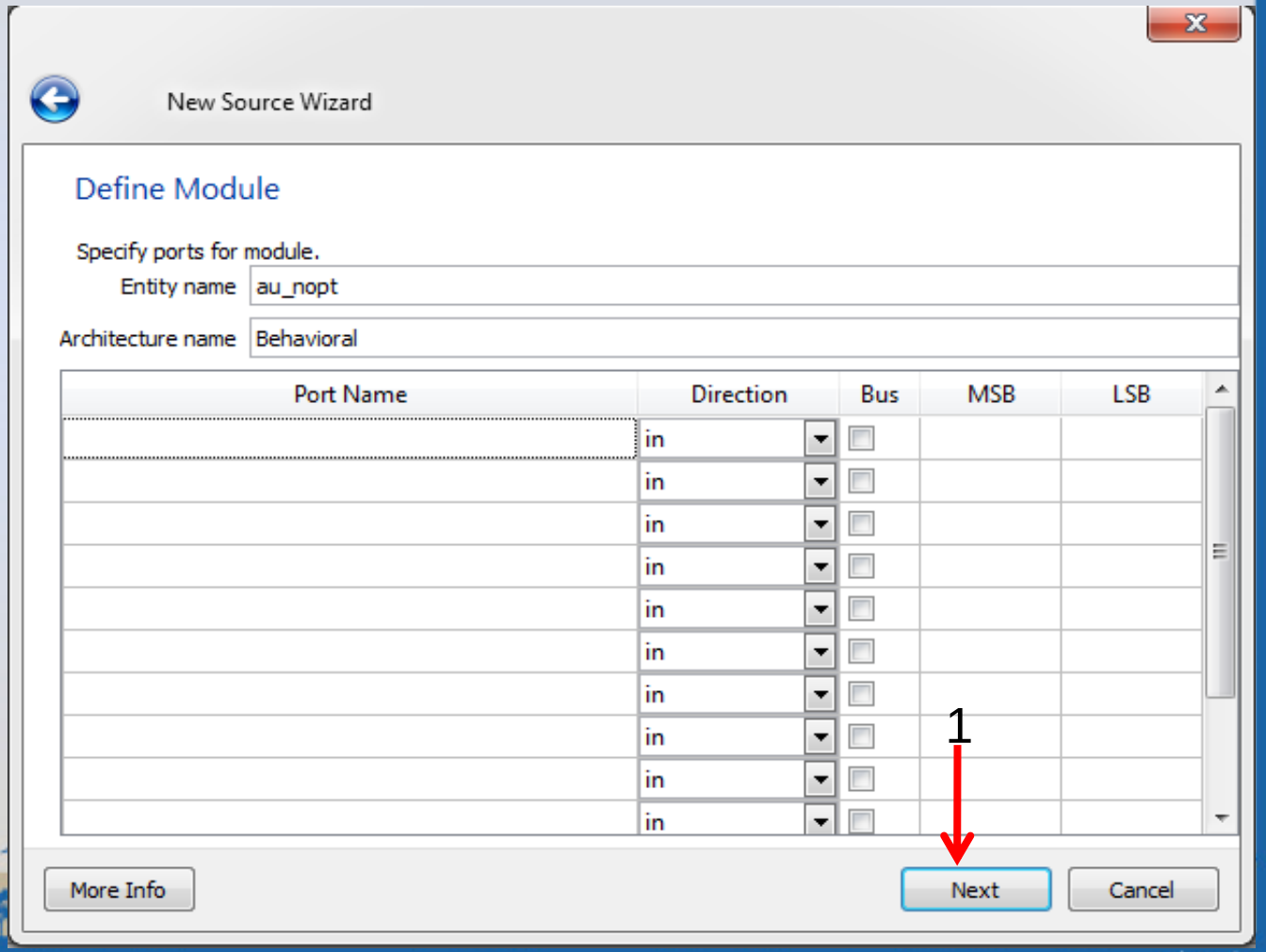
3.Lokacija - neka ostane predložena lokacija

4.Next



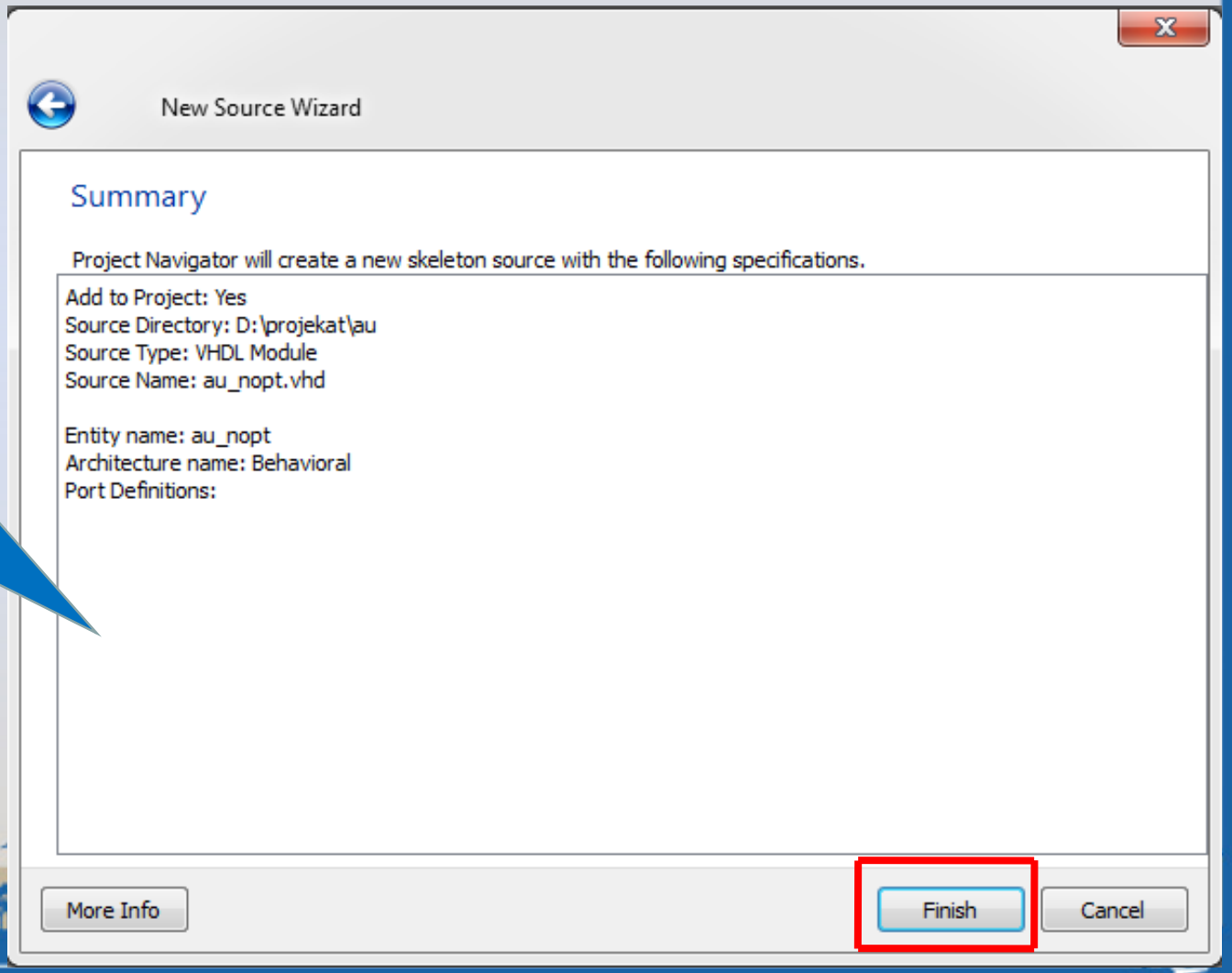
“Prazan” modul

1. Next



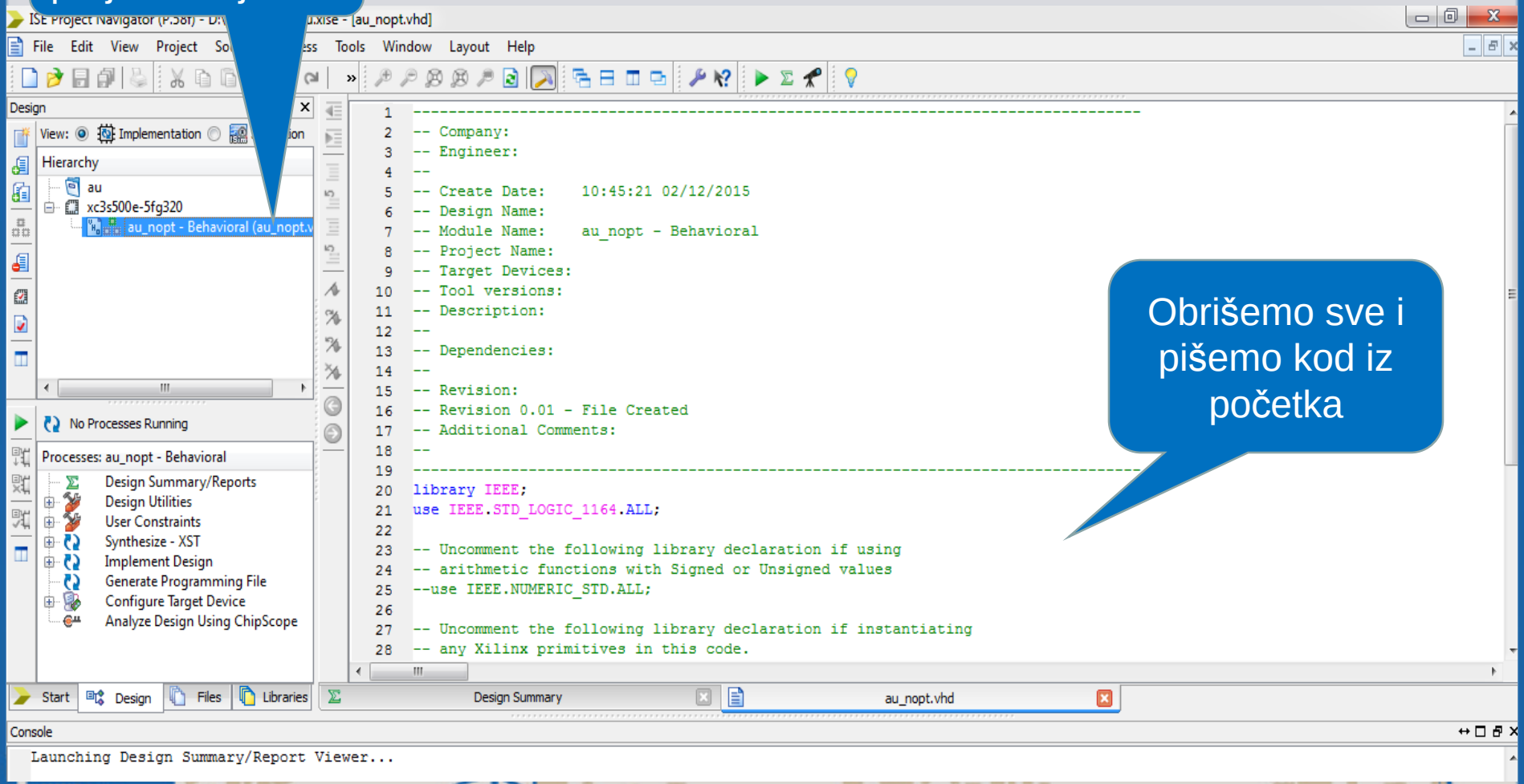
“Prazan” modul

Informativni dijalog o projektnom fajlu, biramo Finish.



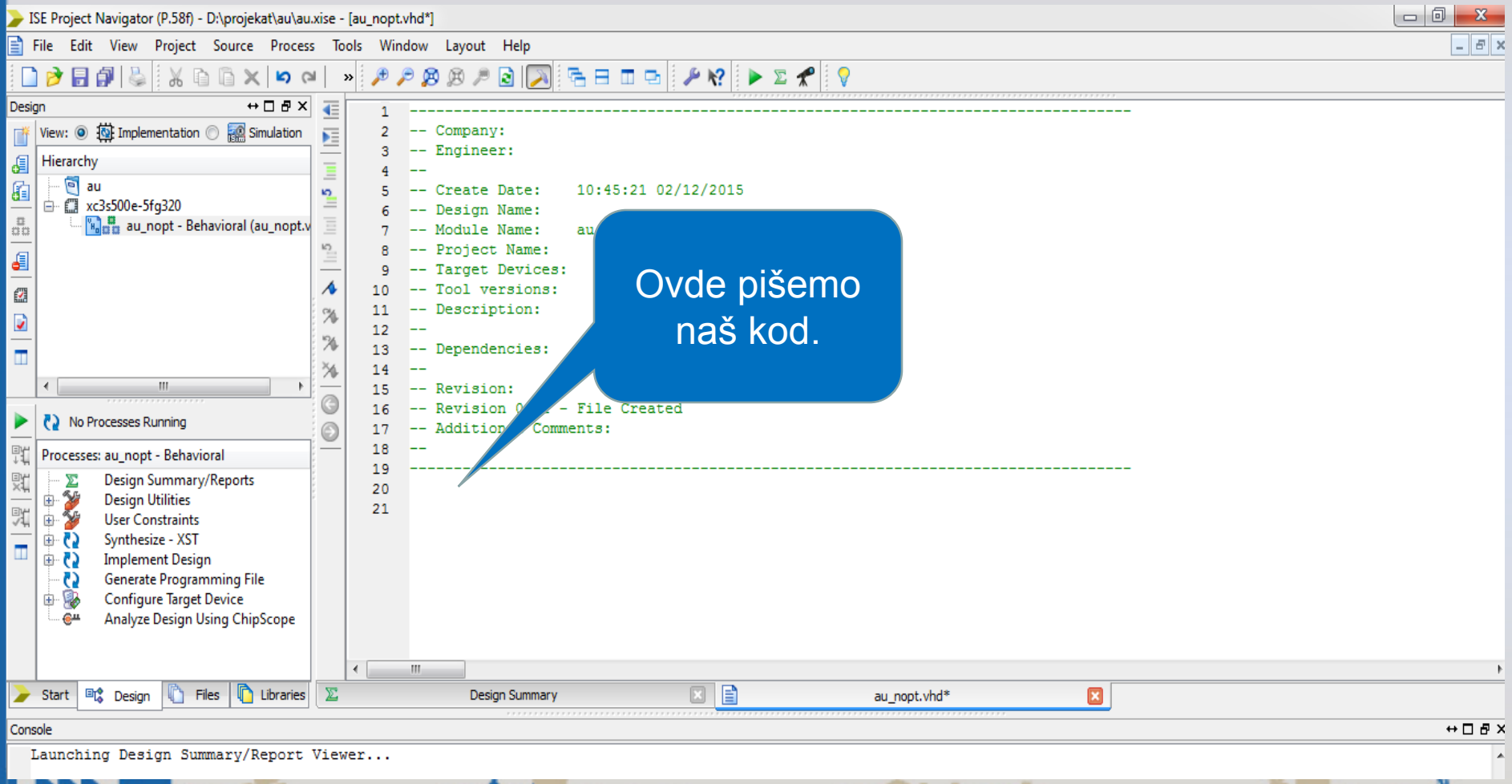
Novi modul - neoptimizovan

Selektovan je projektni fajl.



Obrišemo sve i pišemo kod iz početka

Pisanje neoptimizovanog koda



Neoptimizovana arhitektura - kod

numeric_std

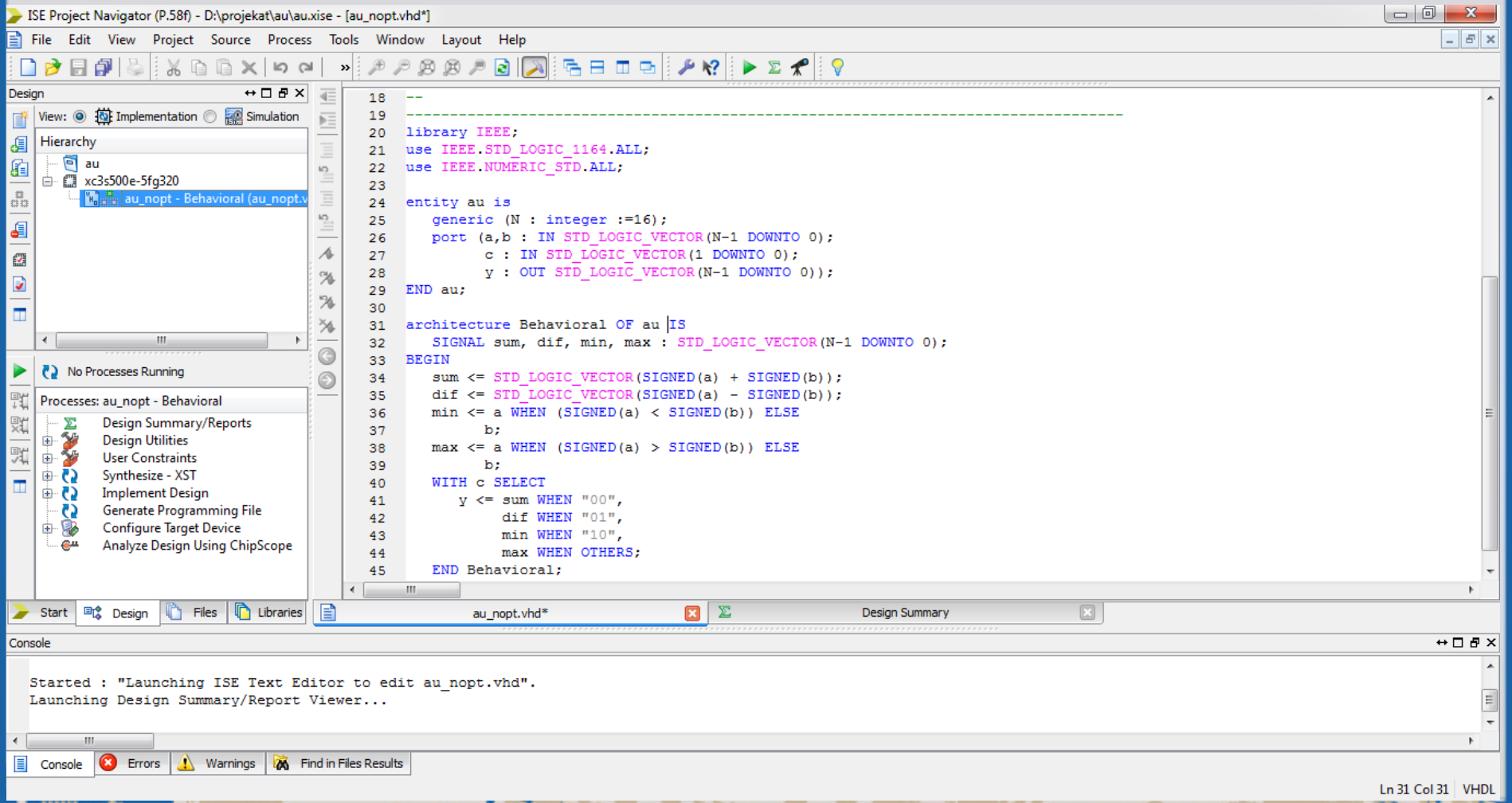
Podrazumeva vrednost generičnog parametra

Neoptimizovana arhitektura

```
18  --
19  ----------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.NUMERIC_STD.ALL;
23
24  entity au is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNTO 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNTO 0));
29  END au;
30
31  architecture Behavioral OF au IS
32     SIGNAL sum, dif, min, max : STD_LOGIC_VECTOR(N-1 DOWNTO 0);
33  BEGIN
34     sum <= STD_LOGIC_VECTOR(SIGNED(a) + SIGNED(b));
35     dif <= STD_LOGIC_VECTOR(SIGNED(a) - SIGNED(b));
36     min <= a WHEN (SIGNED(a) < SIGNED(b)) ELSE
37           b;
38     max <= a WHEN (SIGNED(a) > SIGNED(b)) ELSE
39           b;
40     WITH c SELECT
41        y <= sum WHEN "00",
42             dif WHEN "01",
43             min WHEN "10",
44             max WHEN OTHERS;
45     END Behavioral;
```

Prilikom sisteze koda biće usvojena ova vrednost generičnog parametra

Pisanje koda



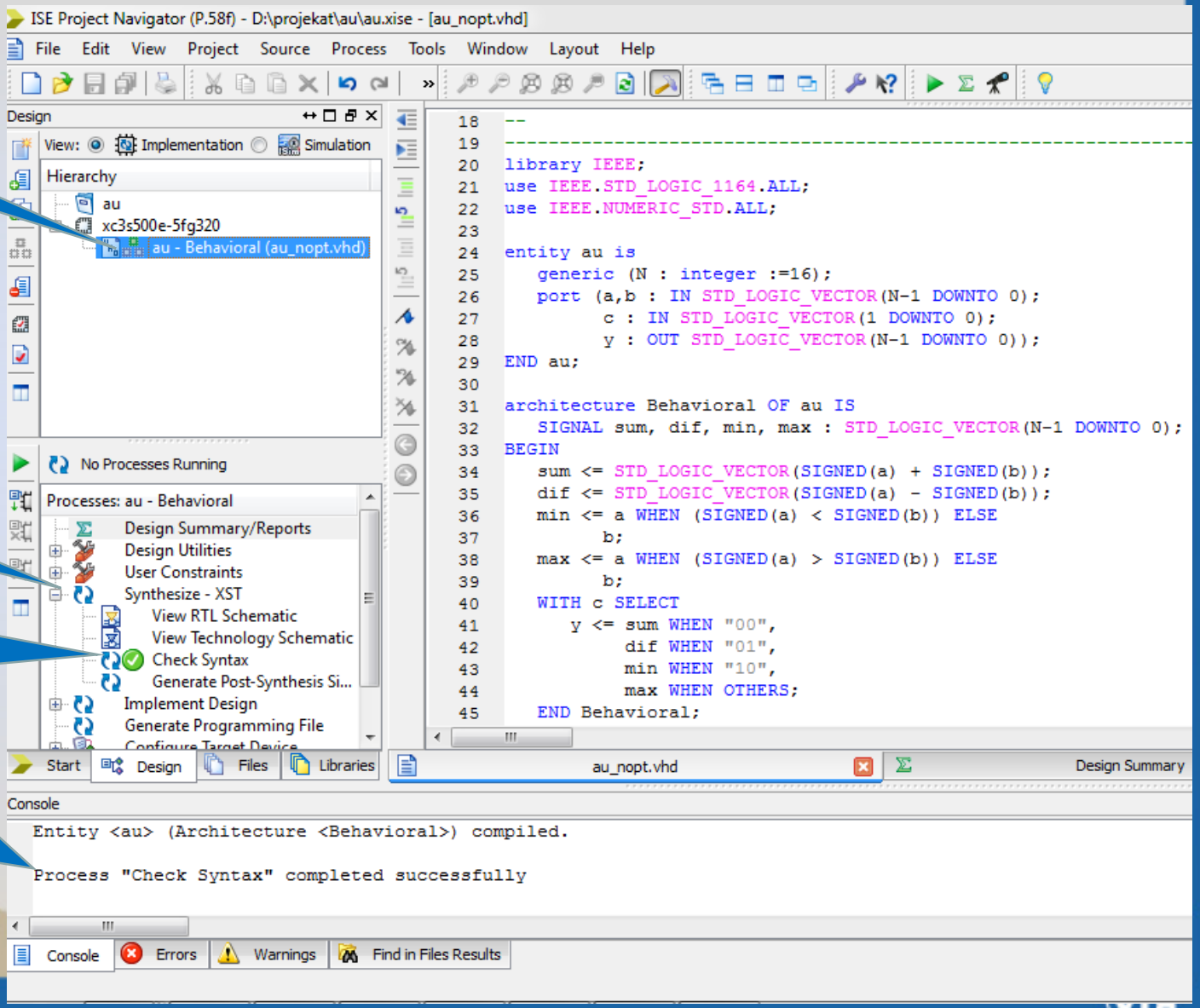
Provera sintakse

Selektovan je projektni fajl.

Klik na + ispred Synthesize -XST

Dvoklik na Check Syntax.

Poruka da nema sintaksnih grešaka



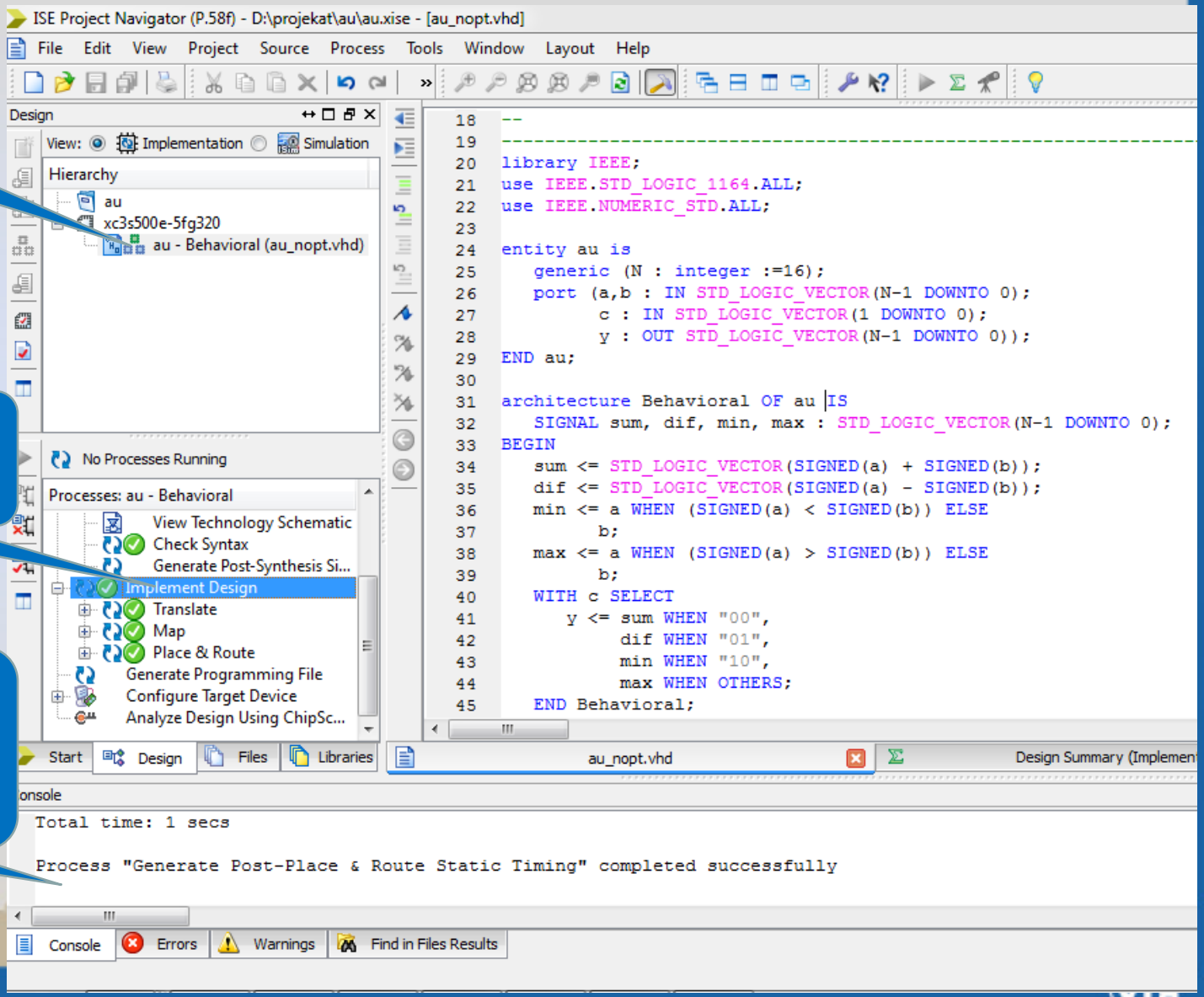

```
18  --
19  ----------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.NUMERIC_STD.ALL;
23
24  entity au is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNTO 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNTO 0));
29  END au;
30
31  architecture Behavioral OF au IS
32     SIGNAL sum, dif, min, max : STD_LOGIC_VECTOR(N-1 DOWNTO 0);
33  BEGIN
34     sum <= STD_LOGIC_VECTOR(SIGNED(a) + SIGNED(b));
35     dif <= STD_LOGIC_VECTOR(SIGNED(a) - SIGNED(b));
36     min <= a WHEN (SIGNED(a) < SIGNED(b)) ELSE
37            b;
38     max <= a WHEN (SIGNED(a) > SIGNED(b)) ELSE
39            b;
40     WITH c SELECT
41        y <= sum WHEN "00",
42             dif WHEN "01",
43             min WHEN "10",
44             max WHEN OTHERS;
45     END Behavioral;
```

Implementacija neoptimizovane arhitekture

Selektovan je projektni fajl.

Dvoklik na Implement Desing.

Poruka da je implementacija uspešno okončana.

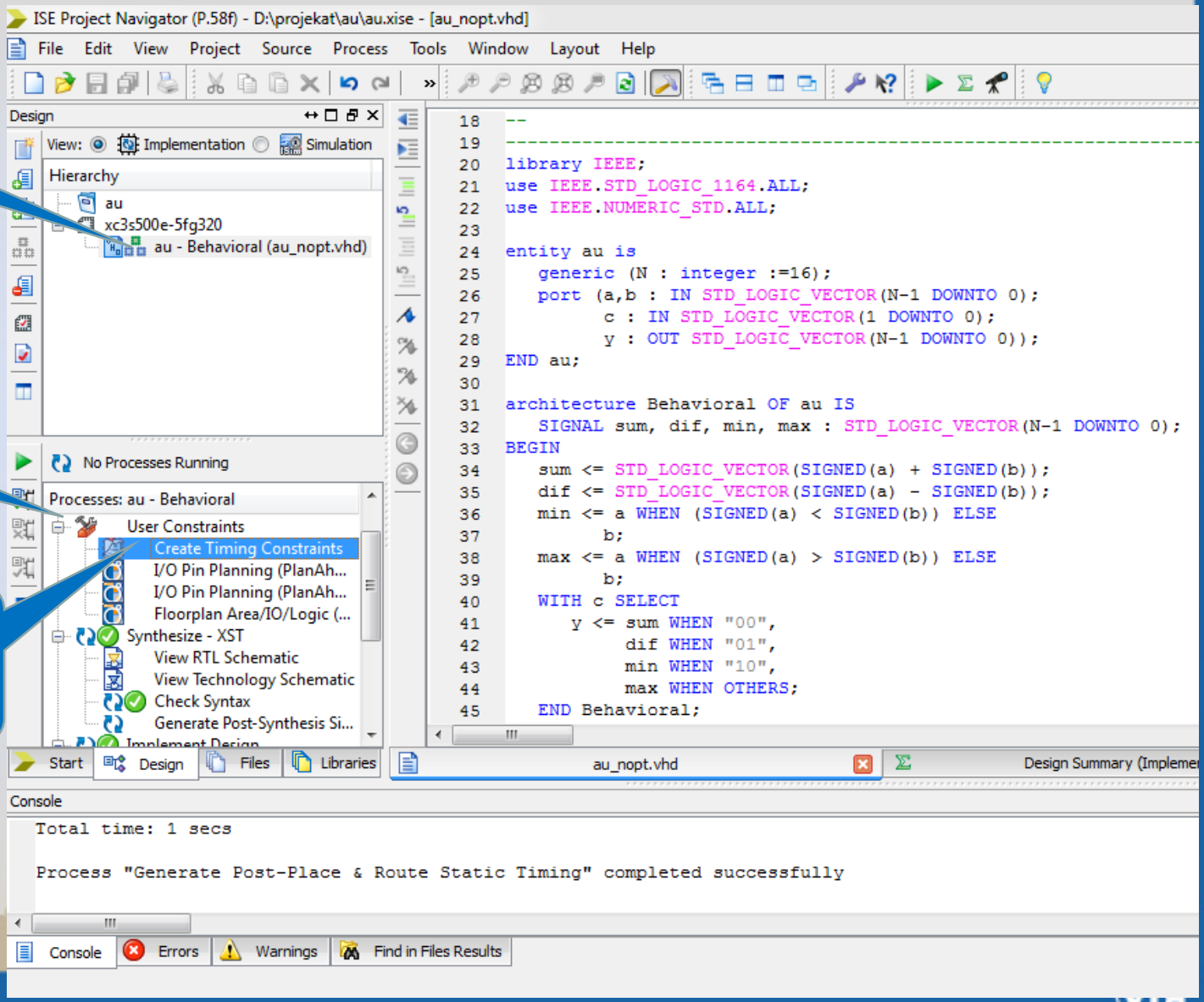


Postavljanje vremenskog ograničenja

Selektovan je projektni fajl.

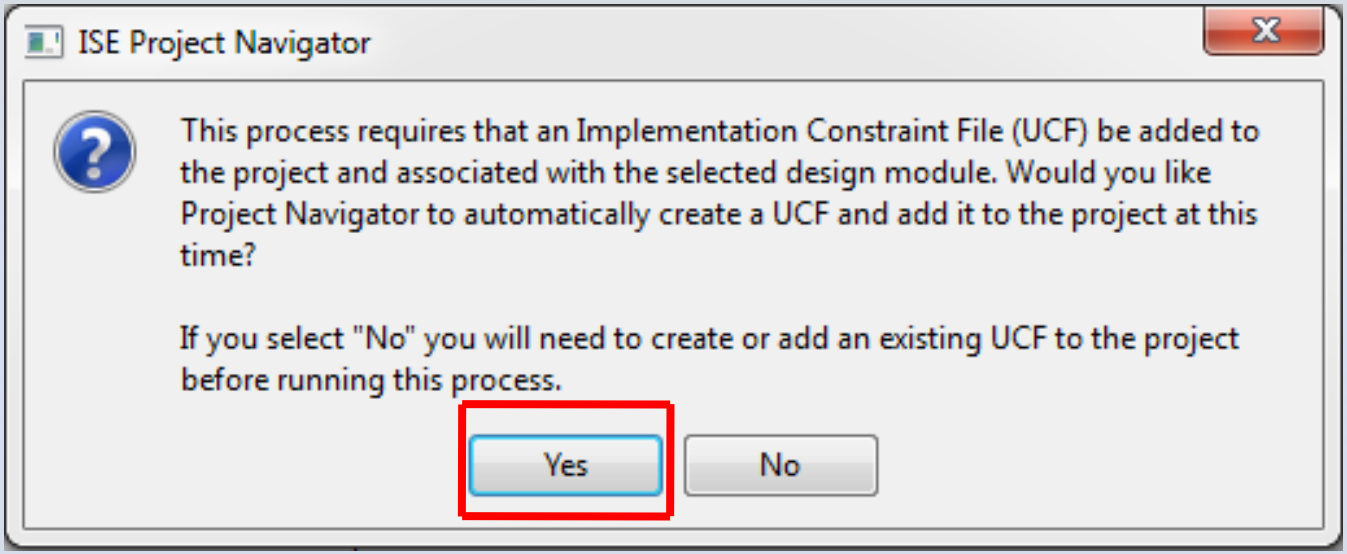
Klik na + ispred User Constraints

Dupli klik preko “Create Timing Constranints”

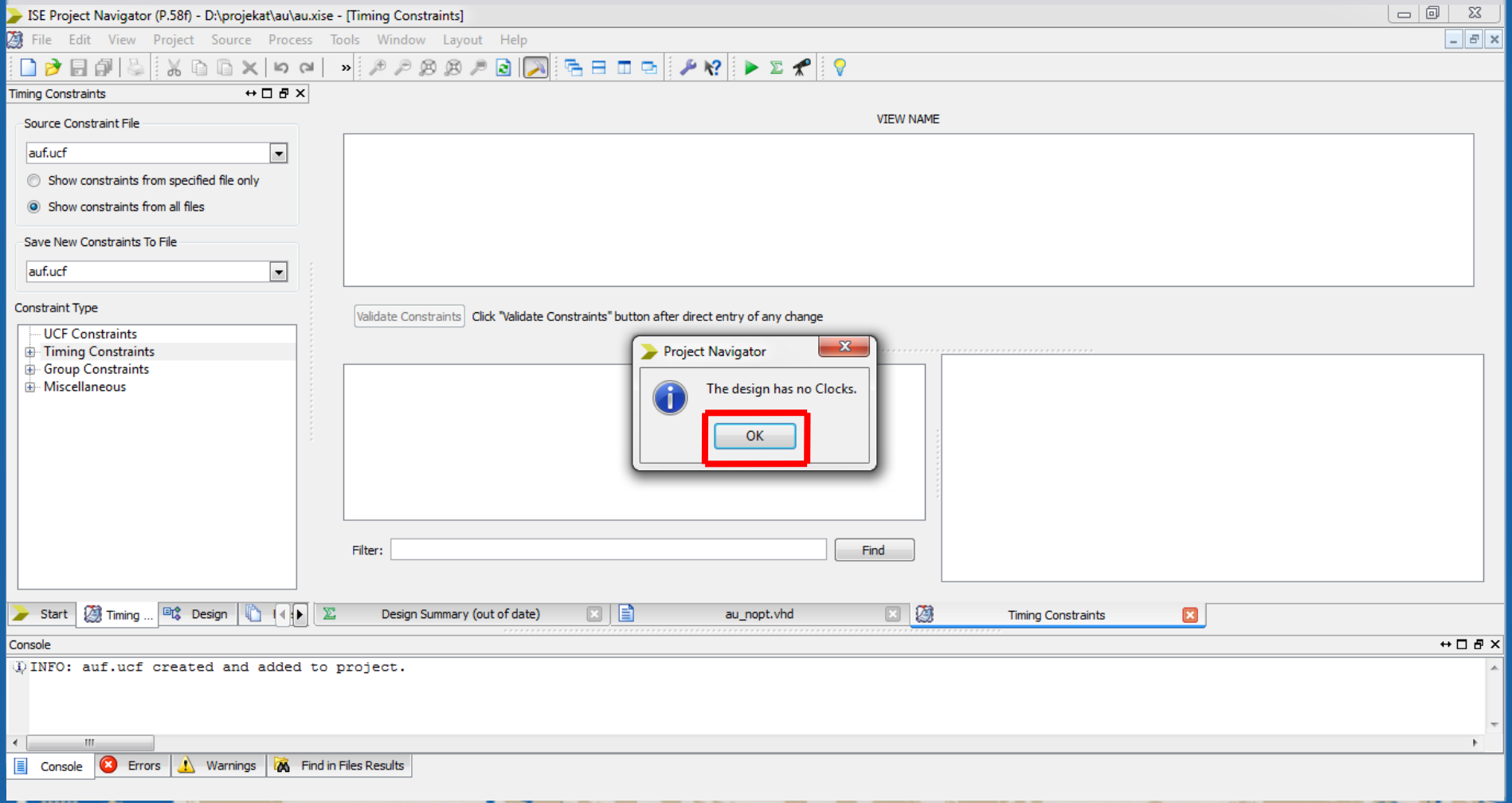



```
18  --
19  ----------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.NUMERIC_STD.ALL;
23
24  entity au is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNTO 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNTO 0));
29  END au;
30
31  architecture Behavioral OF au IS
32     SIGNAL sum, dif, min, max : STD_LOGIC_VECTOR(N-1 DOWNTO 0);
33  BEGIN
34     sum <= STD_LOGIC_VECTOR(SIGNED(a) + SIGNED(b));
35     dif <= STD_LOGIC_VECTOR(SIGNED(a) - SIGNED(b));
36     min <= a WHEN (SIGNED(a) < SIGNED(b)) ELSE
37           b;
38     max <= a WHEN (SIGNED(a) > SIGNED(b)) ELSE
39           b;
40     WITH c SELECT
41        y <= sum WHEN "00",
42             dif WHEN "01",
43             min WHEN "10",
44             max WHEN OTHERS;
45     END Behavioral;
```

Postavljanje vremenskog ograničenja



Postavljanje vremenskog ograničenja

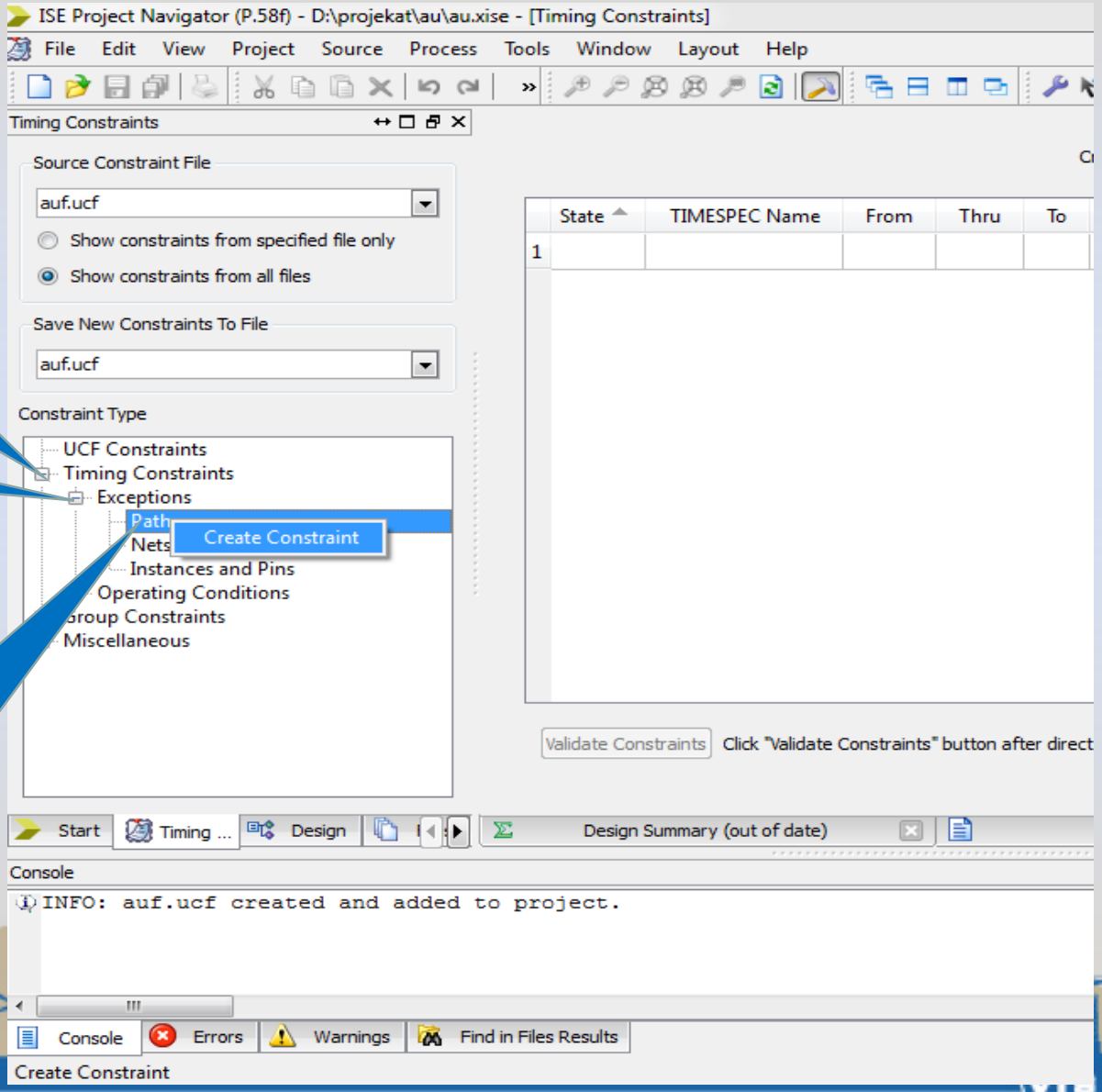


Postavljanje vremenskog ograničenja

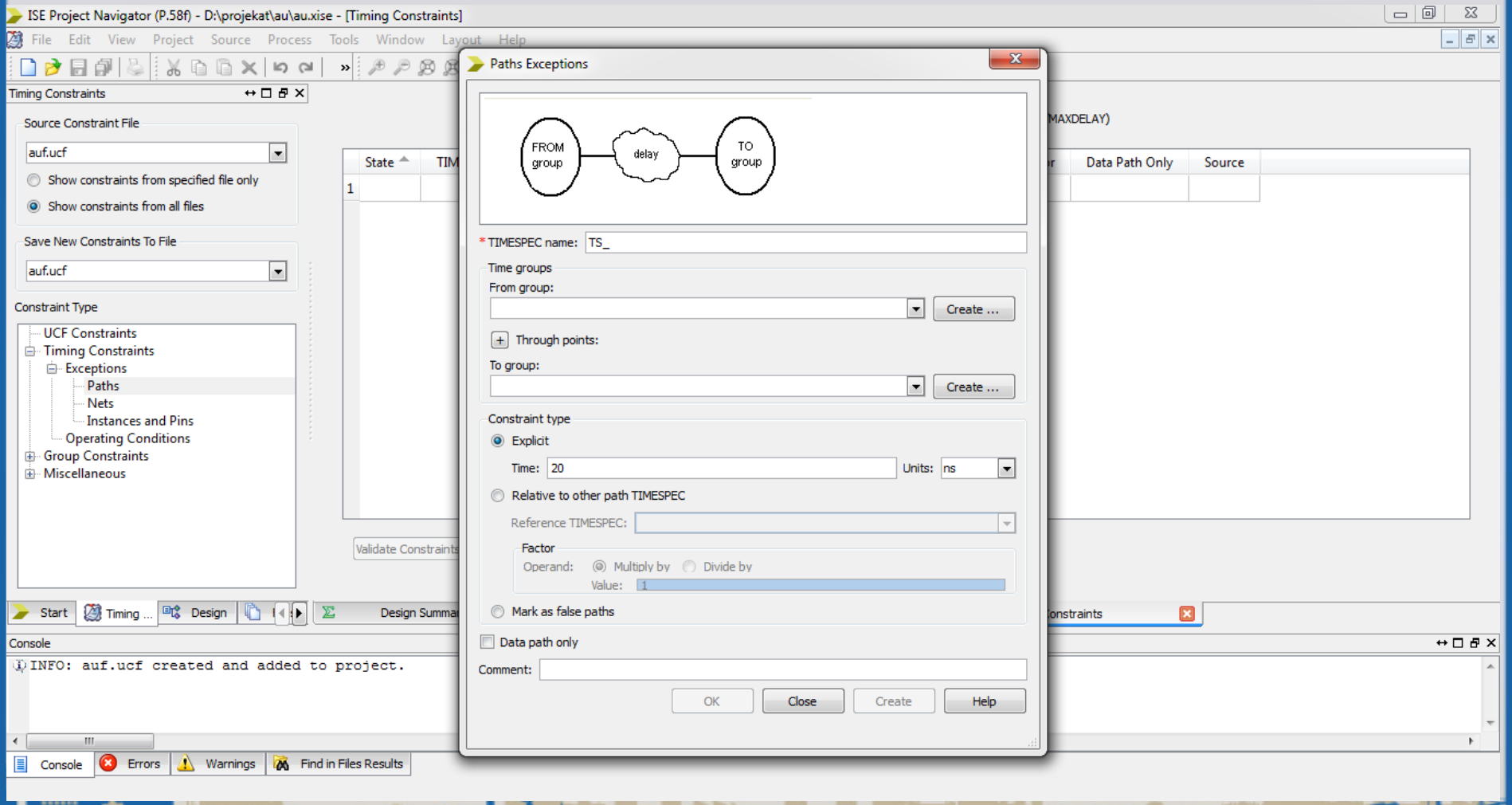
Klik na + ispred Timing Constraints

Klik na + ispred Exceptions

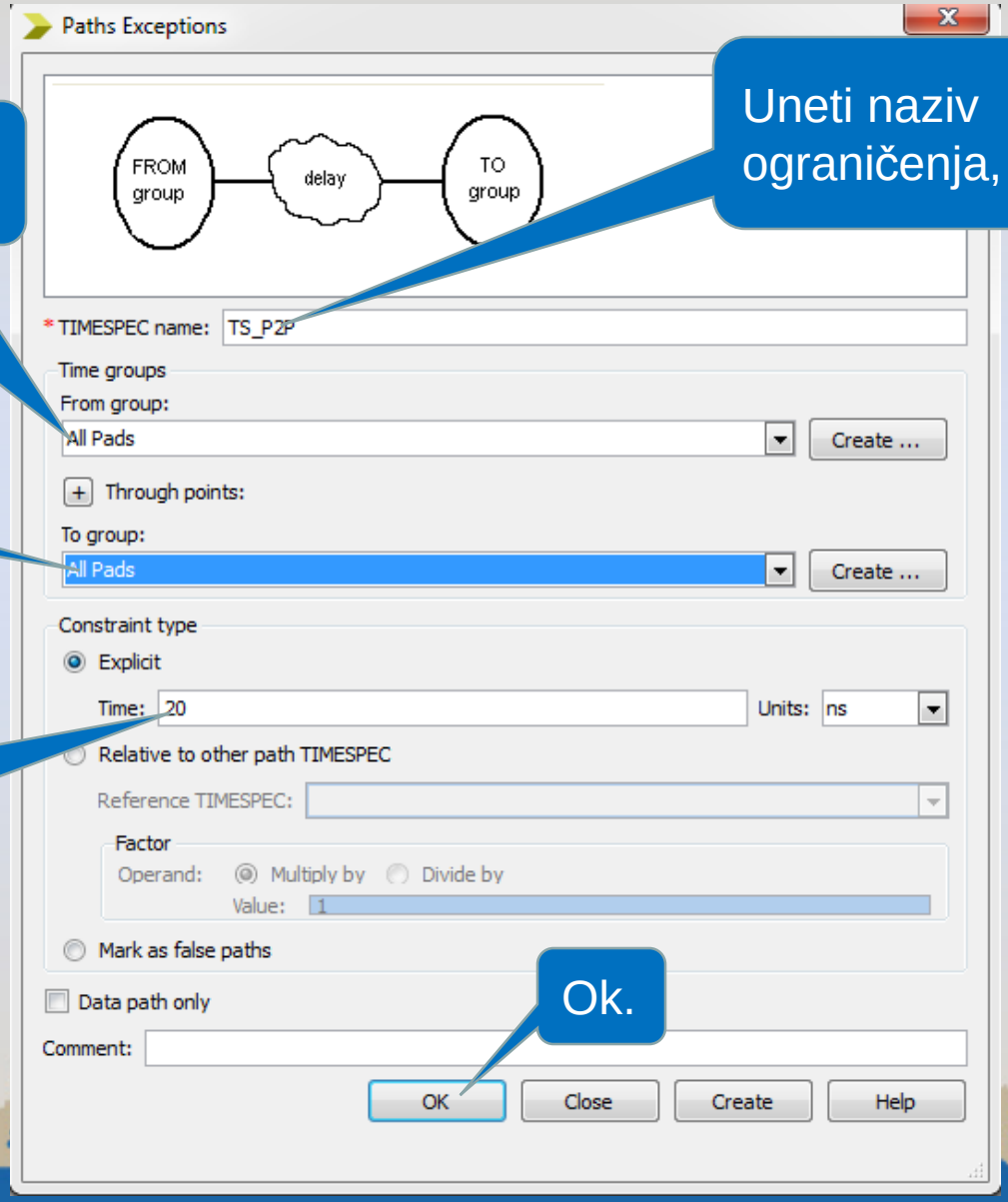
Pritisnite desni taster iznad opcije Paths i izaberite opciju Create Constraint.



Postavljanje vremenskog ograničenja



Postavljanje vremenskog ograničenja



Odabrati All Pads.

Odabrati All Pads.

Upisati 20.

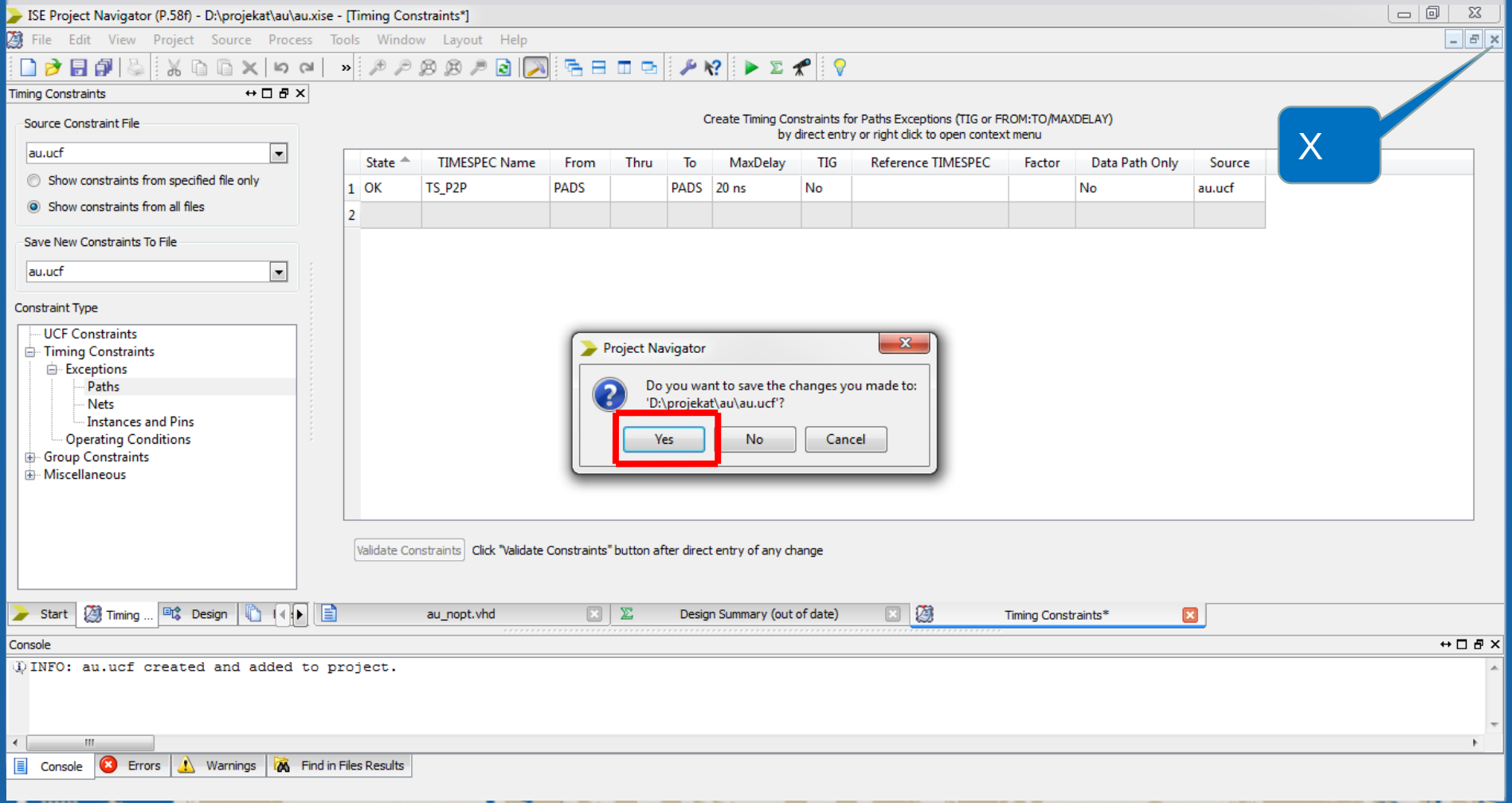
Uneti naziv ograničenja, TS_P2P.

Ok.

Postavljanje vremenskog ograničenja

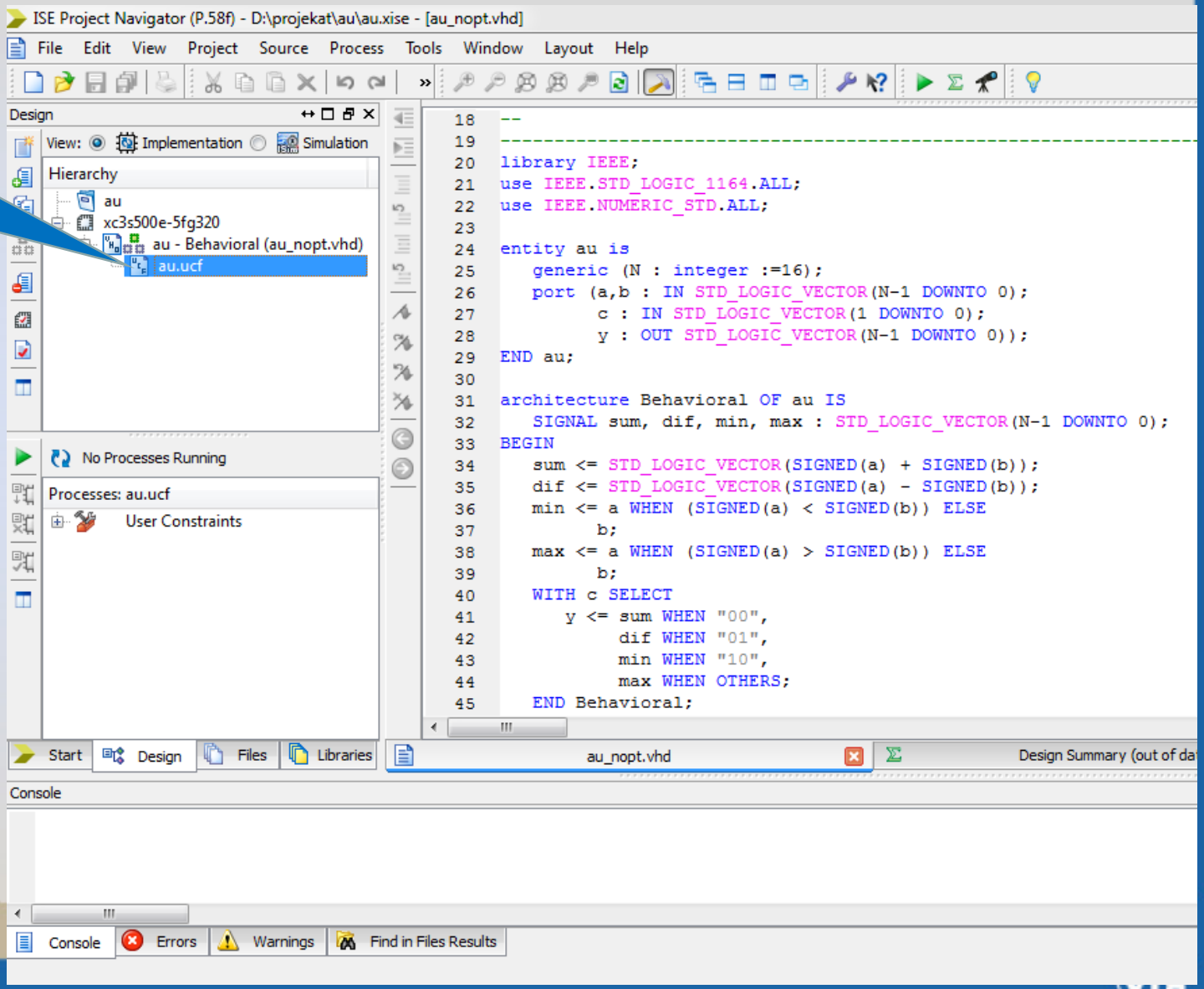
	State	TIMESPEC Name	From	Thru	To	MaxDelay	TIG	Reference TIMESPEC	Factor	Data Path Only	Source
1	OK	TS_P2P	PADS		PADS	20 ns	No			No	au.ucf
2											

Postavljanje vremenskog ograničenja

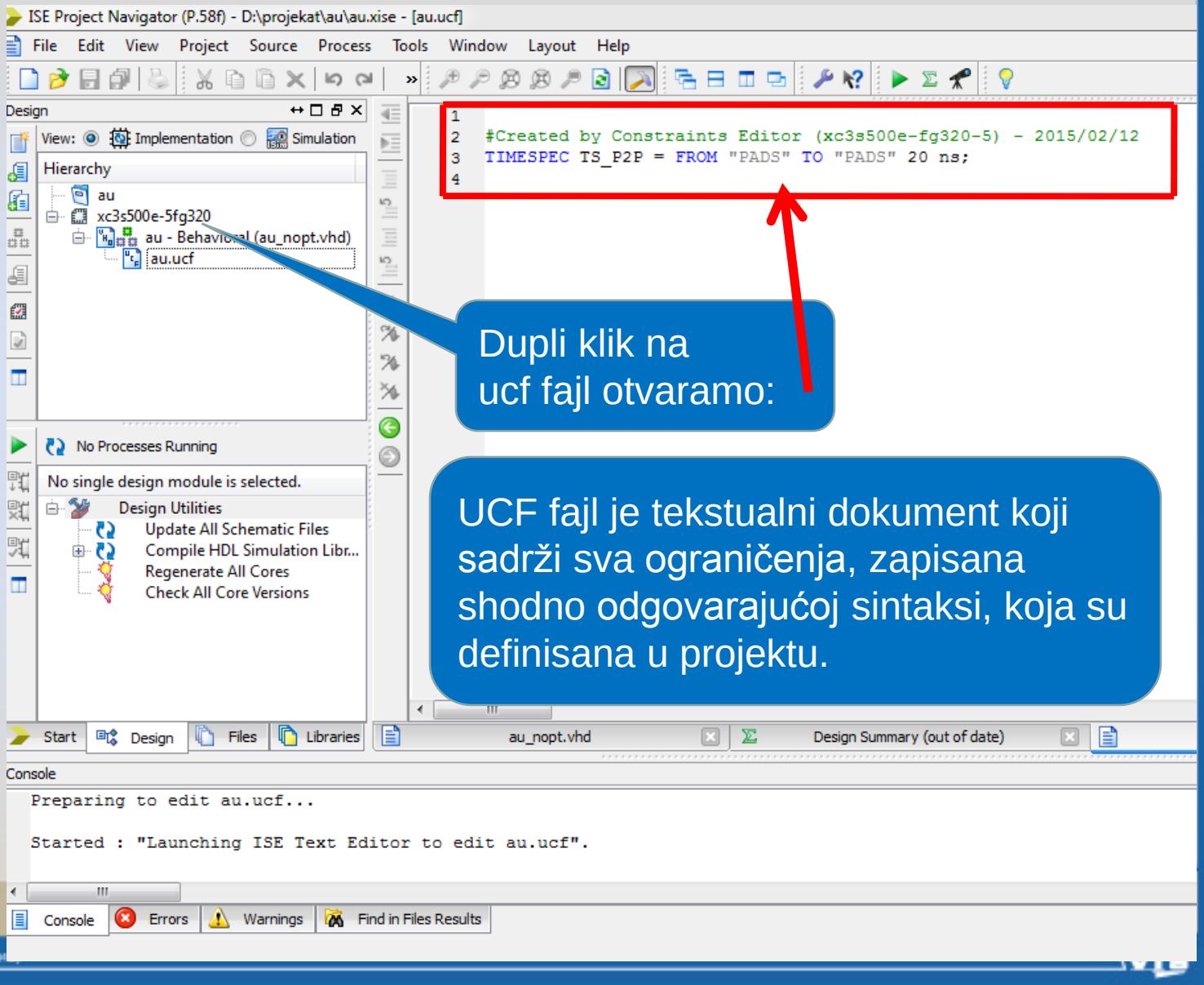


Postavljeno vremensko ograničenje

Kreiran je UCF fajl.

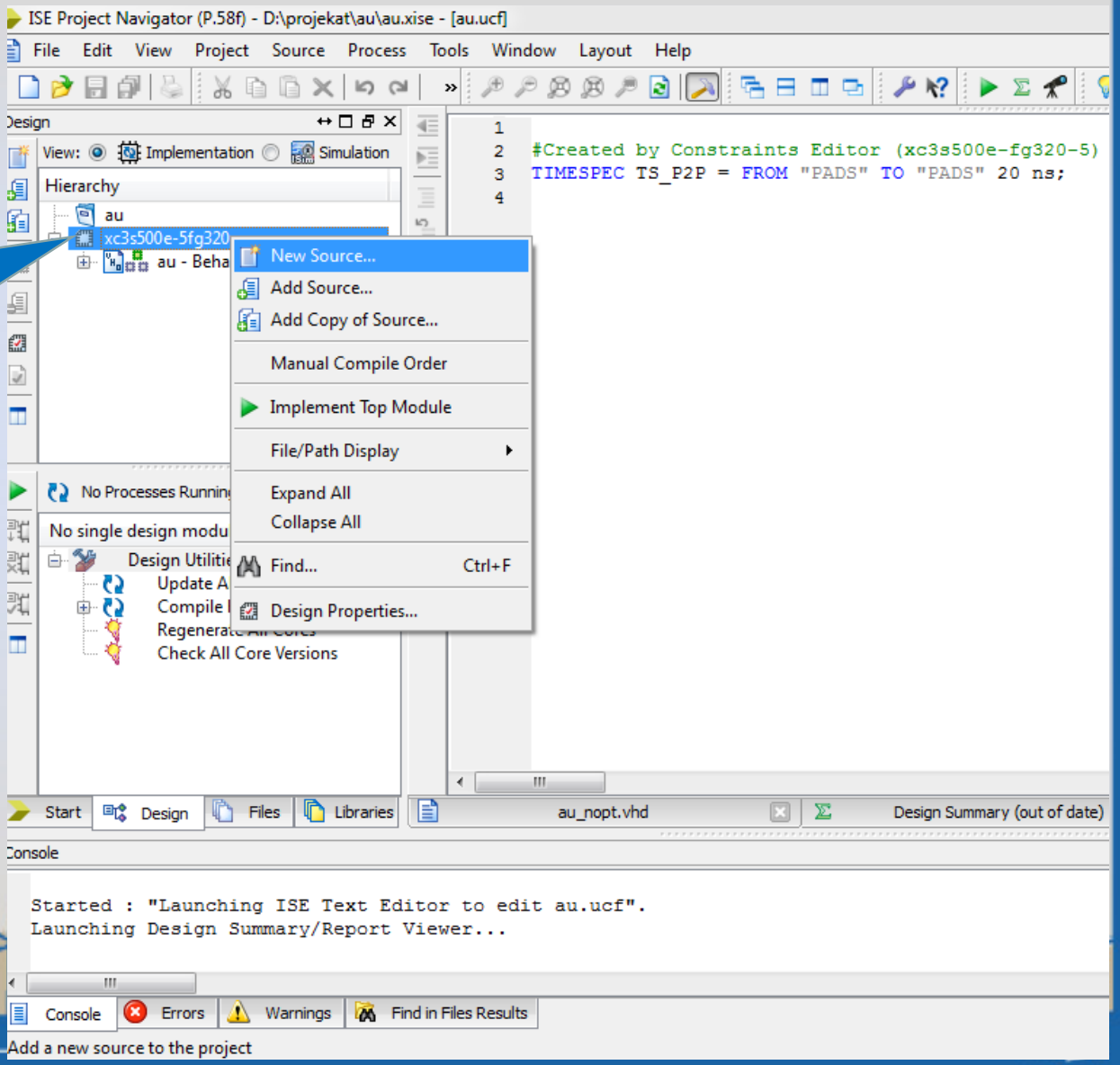


Postavljeno vremensko ograničenje



Kreiranje novog projektnog fajla - optimizovani kod

Desni klik preko oznake kola, a onda New Source.



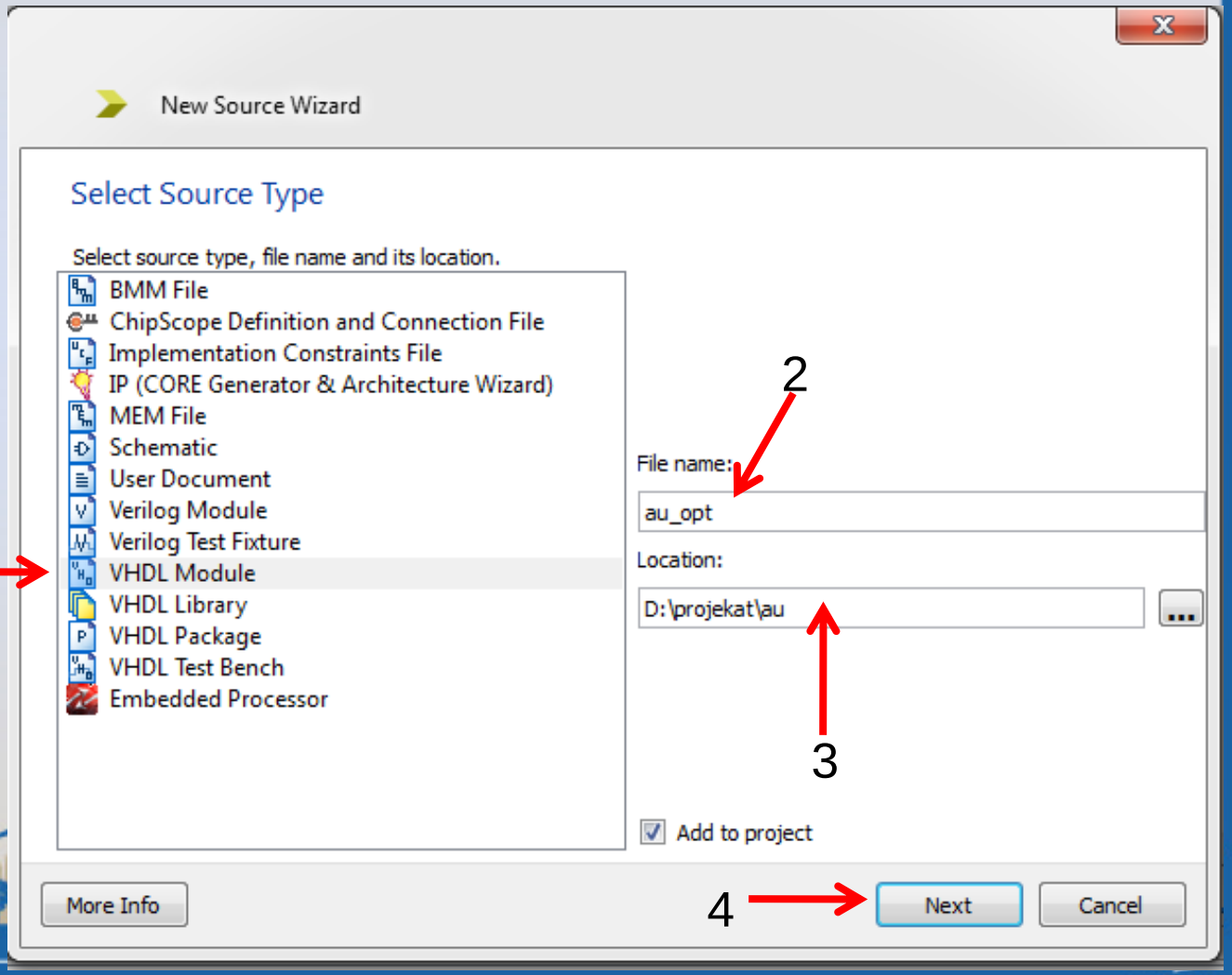
Kreiranje novog projektnog fajla – optimizovani kod

1.Izbor tipa projektnog fajla(biramoVHDL Module)

2.Upišite ime projektnog fajla (neka bude au_opt)

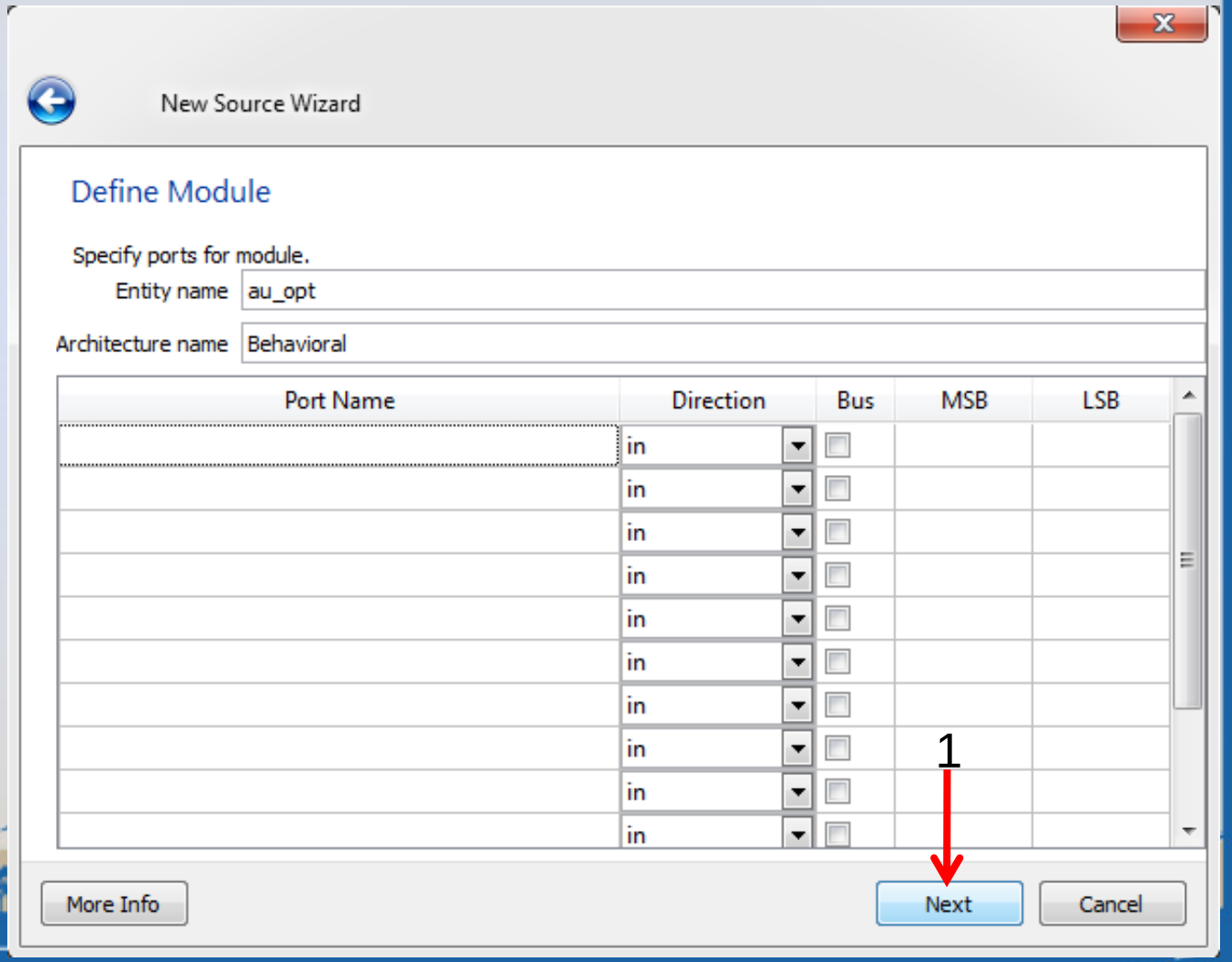
3.Lokacija -neka ostane predložena lokacija

4.Next



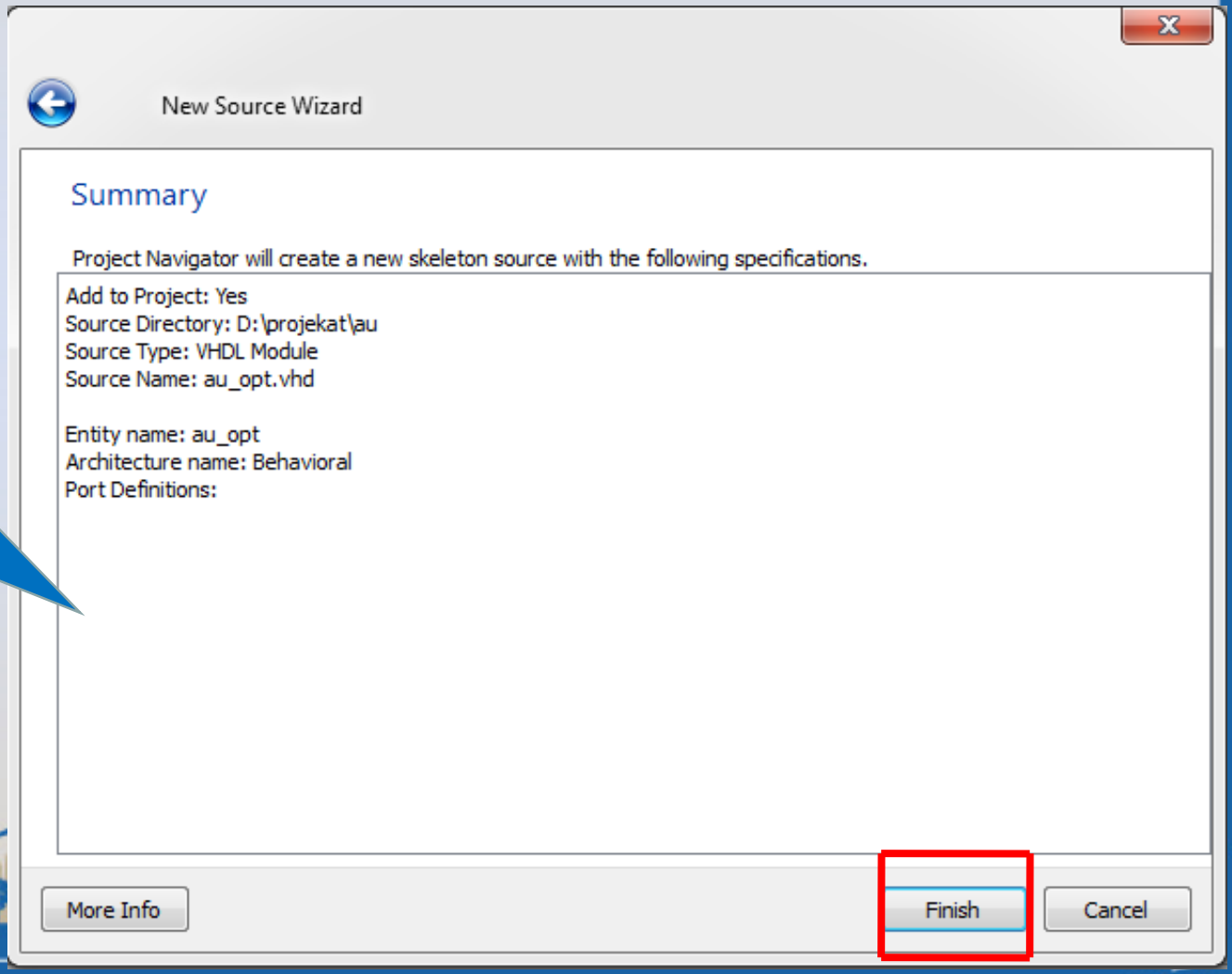
Kreiranje novog projektnog fajla – optimizovani kod

1. Next



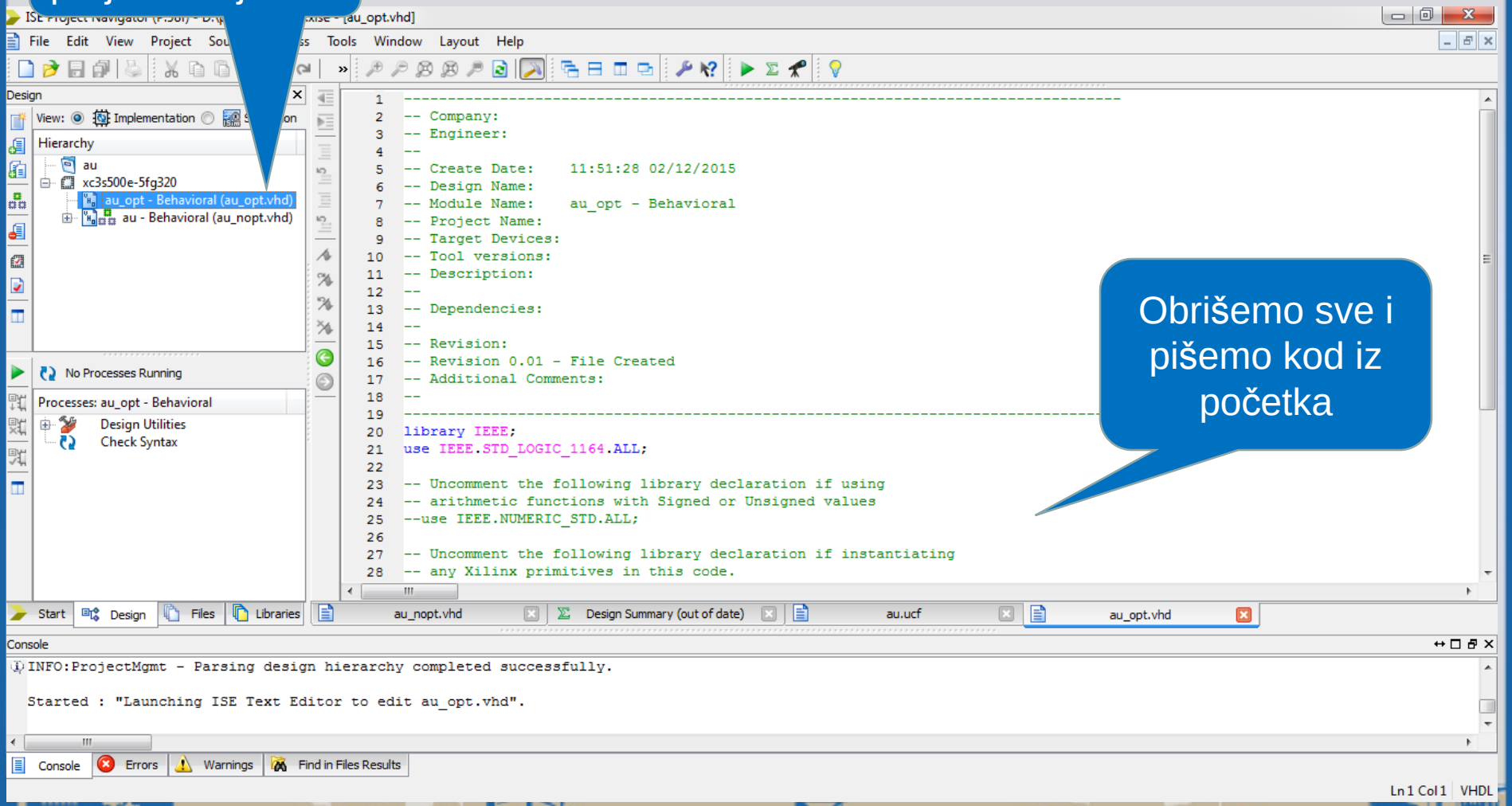
Kreiranje novog projektnog fajla – optimizovani kod

Informativni dijalog o projektnom fajlu, biramo Finish.



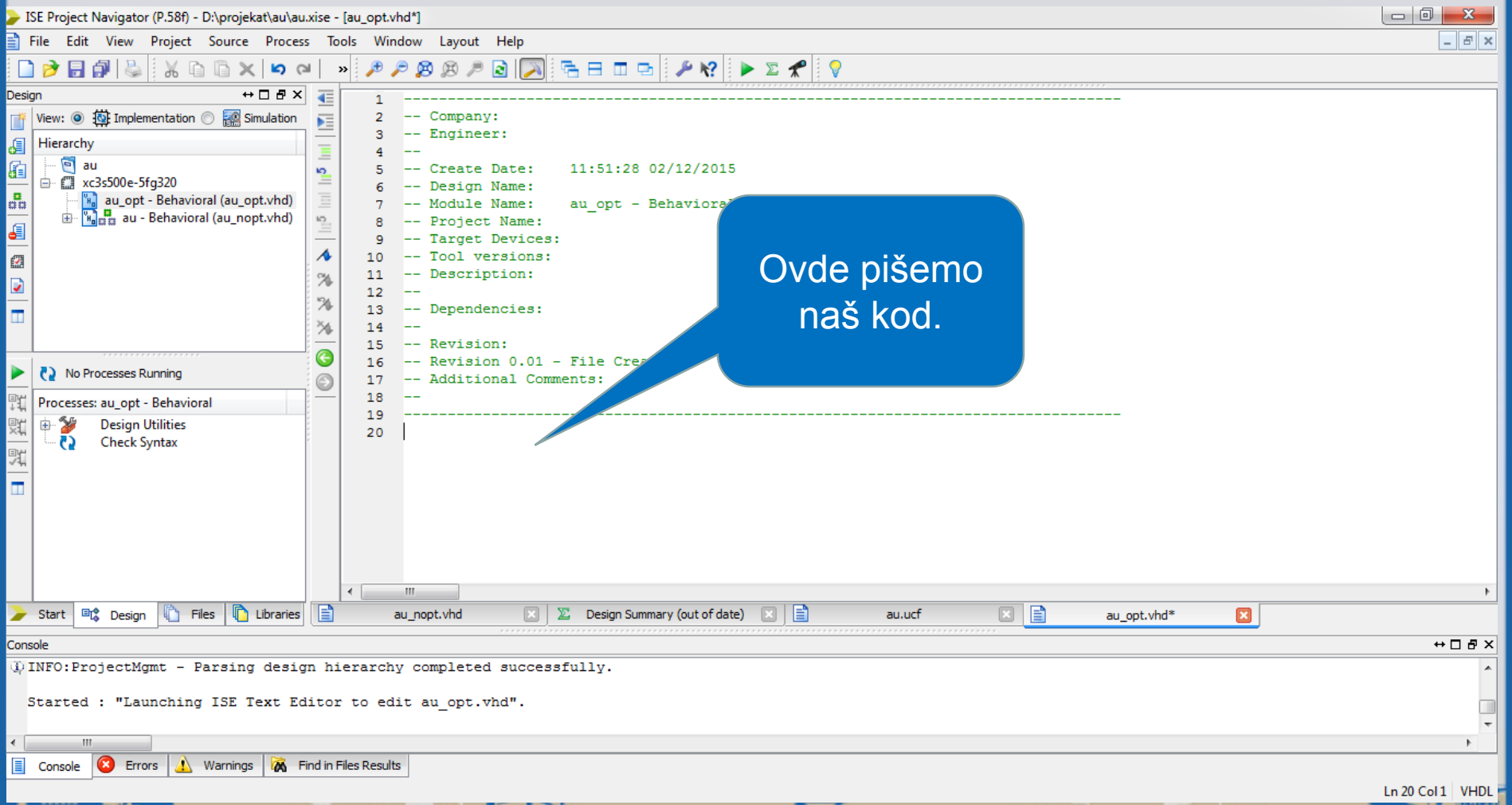
Novi modul – optimizovan kod

Selektovan je projektni fajl.



Obrišemo sve i pišemo kod iz početka

Pisanje optimizovanog koda

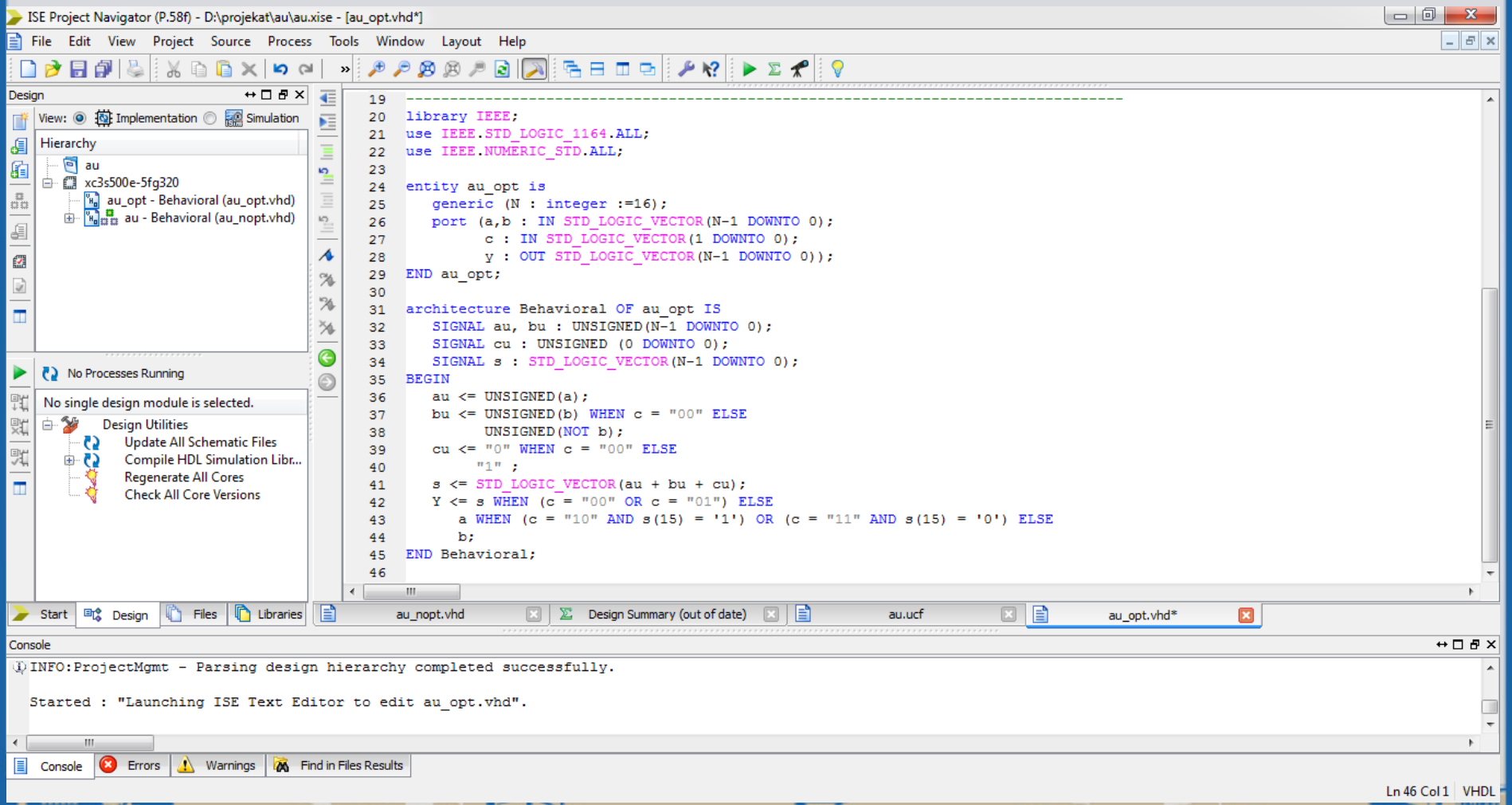


Optimizovana arhitektura - kod

```
19  ----------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.NUMERIC_STD.ALL;
23
24  entity au_opt is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNTO 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNTO 0));
29  END au_opt;
30
31  architecture Behavioral OF au_opt IS
32     SIGNAL au, bu : UNSIGNED(N-1 DOWNTO 0);
33     SIGNAL cu : UNSIGNED (0 DOWNTO 0);
34     SIGNAL s : STD_LOGIC_VECTOR(N-1 DOWNTO 0);
35  BEGIN
36     au <= UNSIGNED(a);
37     bu <= UNSIGNED(b) WHEN c = "00" ELSE
38           UNSIGNED(NOT b);
39     cu <= "0" WHEN c = "00" ELSE
40          "1" ;
41     s <= STD_LOGIC_VECTOR(au + bu + cu);
42     Y <= s WHEN (c = "00" OR c = "01") ELSE
43        a WHEN (c = "10" AND s(15) = '1') OR (c = "11" AND s(15) = '0') ELSE
44        b;
45  END Behavioral;
46
```

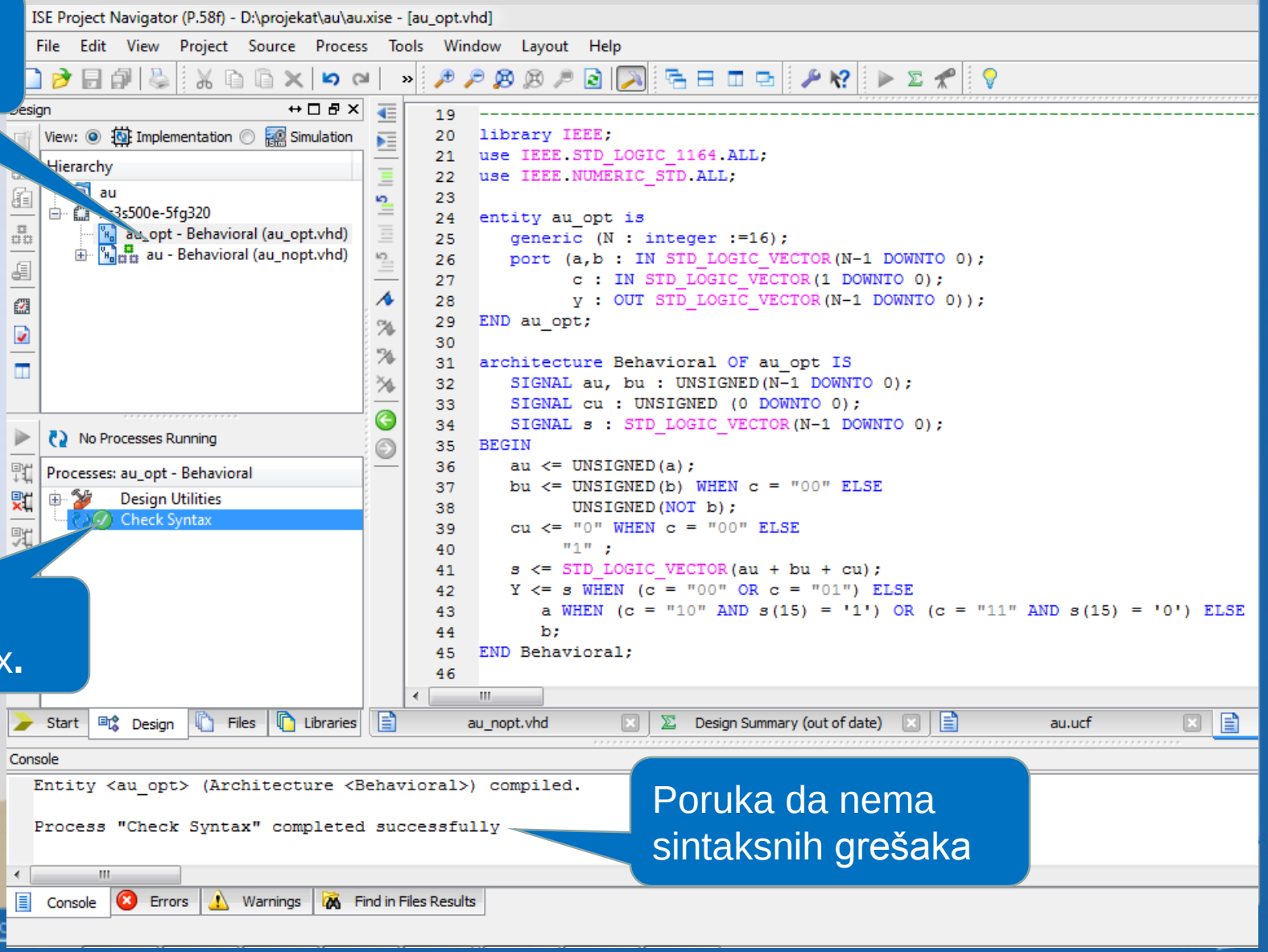
Prilikom sisteze koda biće usvojena ova vrednost generičnog parametra

Pisanje optimizovanog koda



Provera sintakse

Selektovan je projektni fajl.




```
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.NUMERIC_STD.ALL;
23
24  entity au_opt is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNTO 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNTO 0));
29  END au_opt;
30
31  architecture Behavioral OF au_opt IS
32     SIGNAL au, bu : UNSIGNED(N-1 DOWNTO 0);
33     SIGNAL cu : UNSIGNED (0 DOWNTO 0);
34     SIGNAL s : STD_LOGIC_VECTOR(N-1 DOWNTO 0);
35  BEGIN
36     au <= UNSIGNED(a);
37     bu <= UNSIGNED(b) WHEN c = "00" ELSE
38           UNSIGNED(NOT b);
39     cu <= "0" WHEN c = "00" ELSE
40           "1" ;
41     s <= STD_LOGIC_VECTOR(au + bu + cu);
42     Y <= s WHEN (c = "00" OR c = "01") ELSE
43        a WHEN (c = "10" AND s(15) = '1') OR (c = "11" AND s(15) = '0') ELSE
44        b;
45  END Behavioral;
46
```

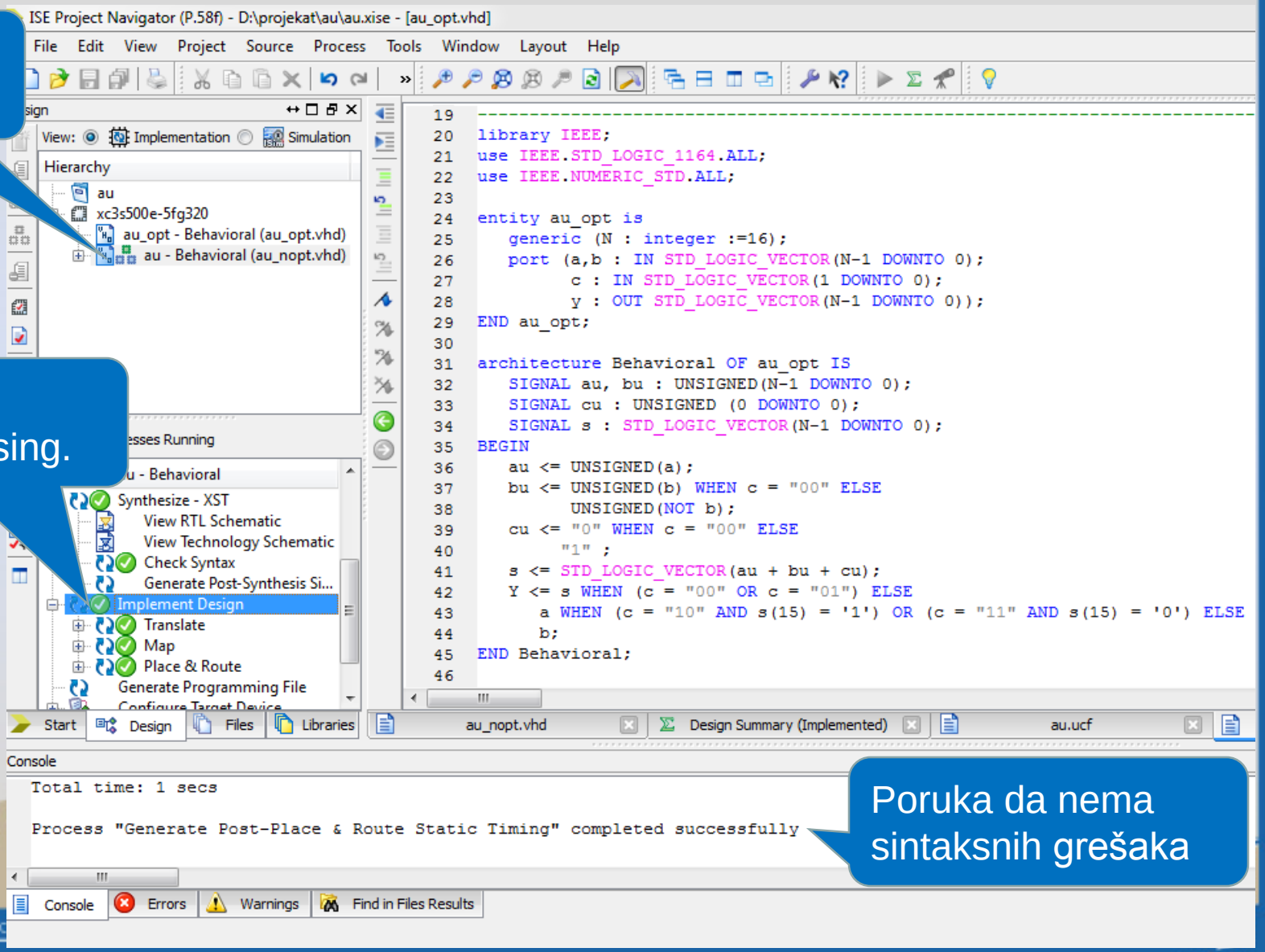
Dvoklik na Check Syntax.

Poruka da nema sintaksnih grešaka

Implementacija optimizovane arhitekture

Selektovan je projektni fajl.

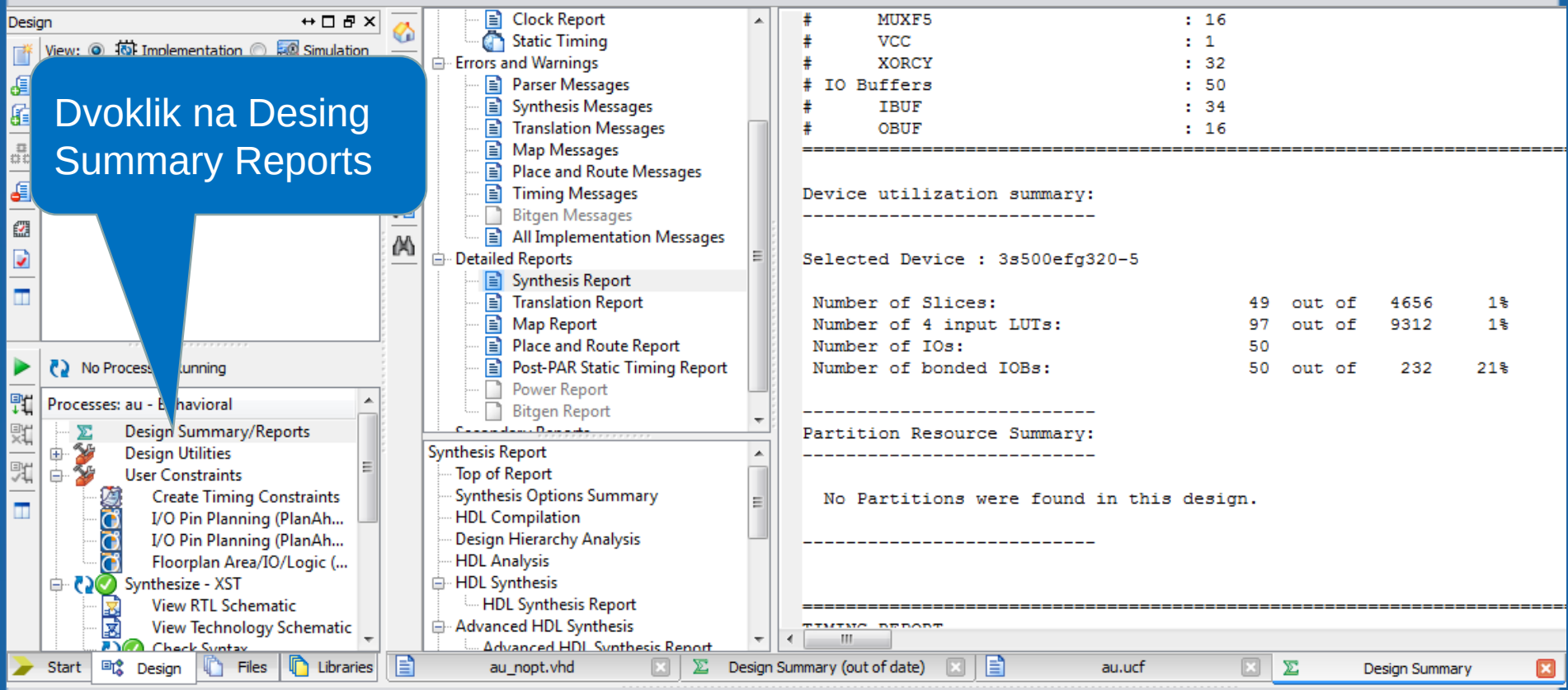
Dvoklik na Implement Desing.



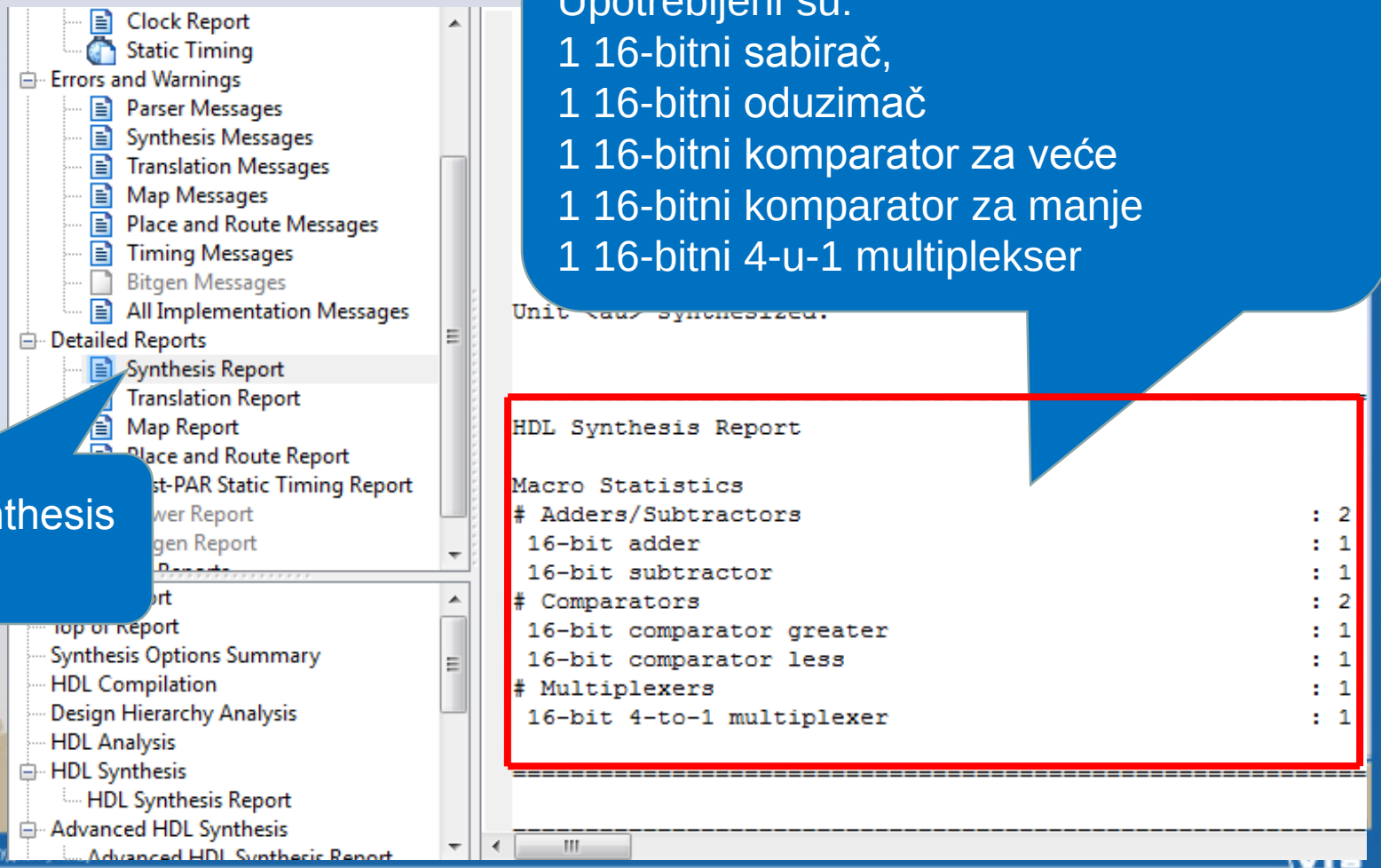

```
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.NUMERIC_STD.ALL;
23
24  entity au_opt is
25     generic (N : integer :=16);
26     port (a,b : IN STD_LOGIC_VECTOR(N-1 DOWNTO 0);
27           c : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
28           y : OUT STD_LOGIC_VECTOR(N-1 DOWNTO 0));
29  END au_opt;
30
31  architecture Behavioral OF au_opt IS
32     SIGNAL au, bu : UNSIGNED(N-1 DOWNTO 0);
33     SIGNAL cu : UNSIGNED (0 DOWNTO 0);
34     SIGNAL s : STD_LOGIC_VECTOR(N-1 DOWNTO 0);
35  BEGIN
36     au <= UNSIGNED(a);
37     bu <= UNSIGNED(b) WHEN c = "00" ELSE
38           UNSIGNED(NOT b);
39     cu <= "0" WHEN c = "00" ELSE
40           "1" ;
41     s <= STD_LOGIC_VECTOR(au + bu + cu);
42     Y <= s WHEN (c = "00" OR c = "01") ELSE
43        a WHEN (c = "10" AND s(15) = '1') OR (c = "11" AND s(15) = '0') ELSE
44        b;
45  END Behavioral;
46
```

Poruka da nema sintaksnih grešaka

Izveštaj o sintezi – neoptimizovan kod



Izveštaj o sintezi – neoptimizovan kod

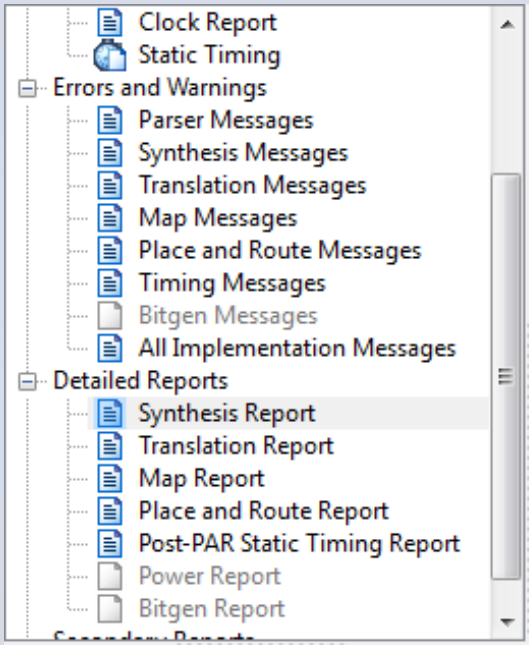


Upotrebljeni su:
1 16-bitni sabirač,
1 16-bitni oduzimač
1 16-bitni komparator za veće
1 16-bitni komparator za manje
1 16-bitni 4-u-1 multiplekser

Dvoklik na “Synthesis Report”.

Izveštaj o sintezi – neoptimizovan kod

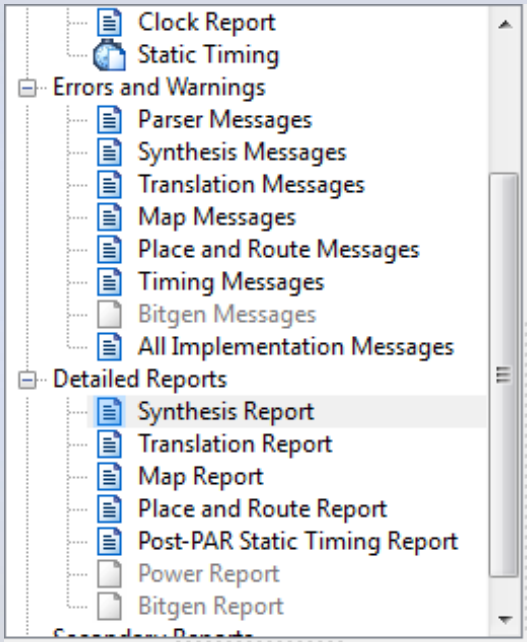
Za realizaciju kola u FPGA potreba su 49 slajsa sa iskorišćenih 97 LUT. Broj potrebnih pinova je 50.

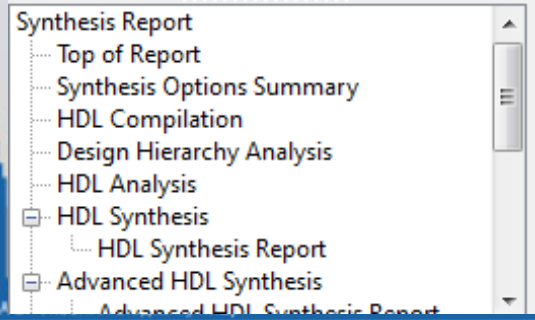


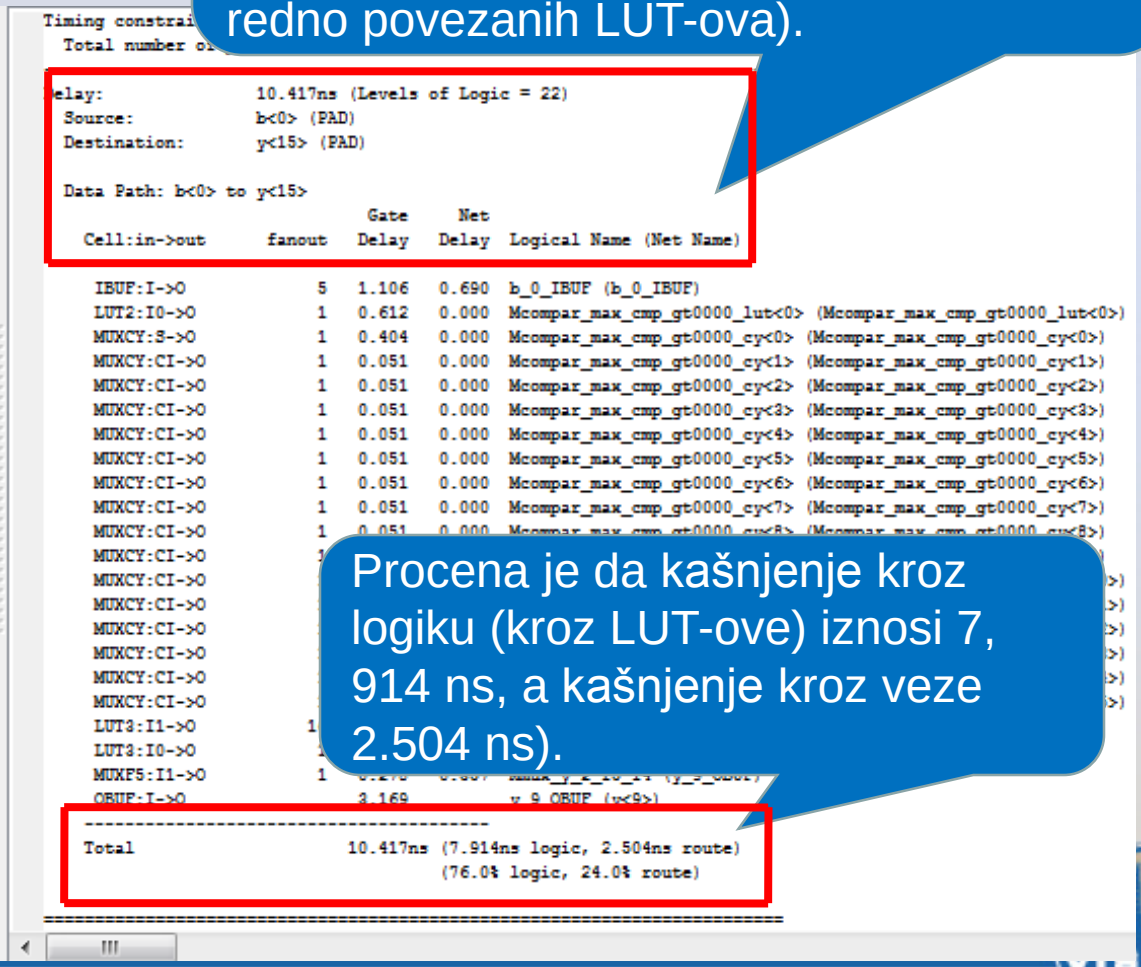

```
#      IBUF
#      OBUF
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s500efg320-5

 Number of Slices:                       49  out of   4656     1%
 Number of 4 input LUTs:                 97  out of   9312     1%
 Number of IOs:                          50
 Number of bonded IOBs:                  50  out of    232    21%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
```

Izveštaj o sintezi – neoptimizovan kod

Maksimalno propagaciono kašnjenje iznosi 10.417 ns i odgovara kašnjenju signala od ulaza b(0) do izlaza y(15). Na toj putanju se nalazi 22 nivoa logike –22 redno povezanih LUT-ova).

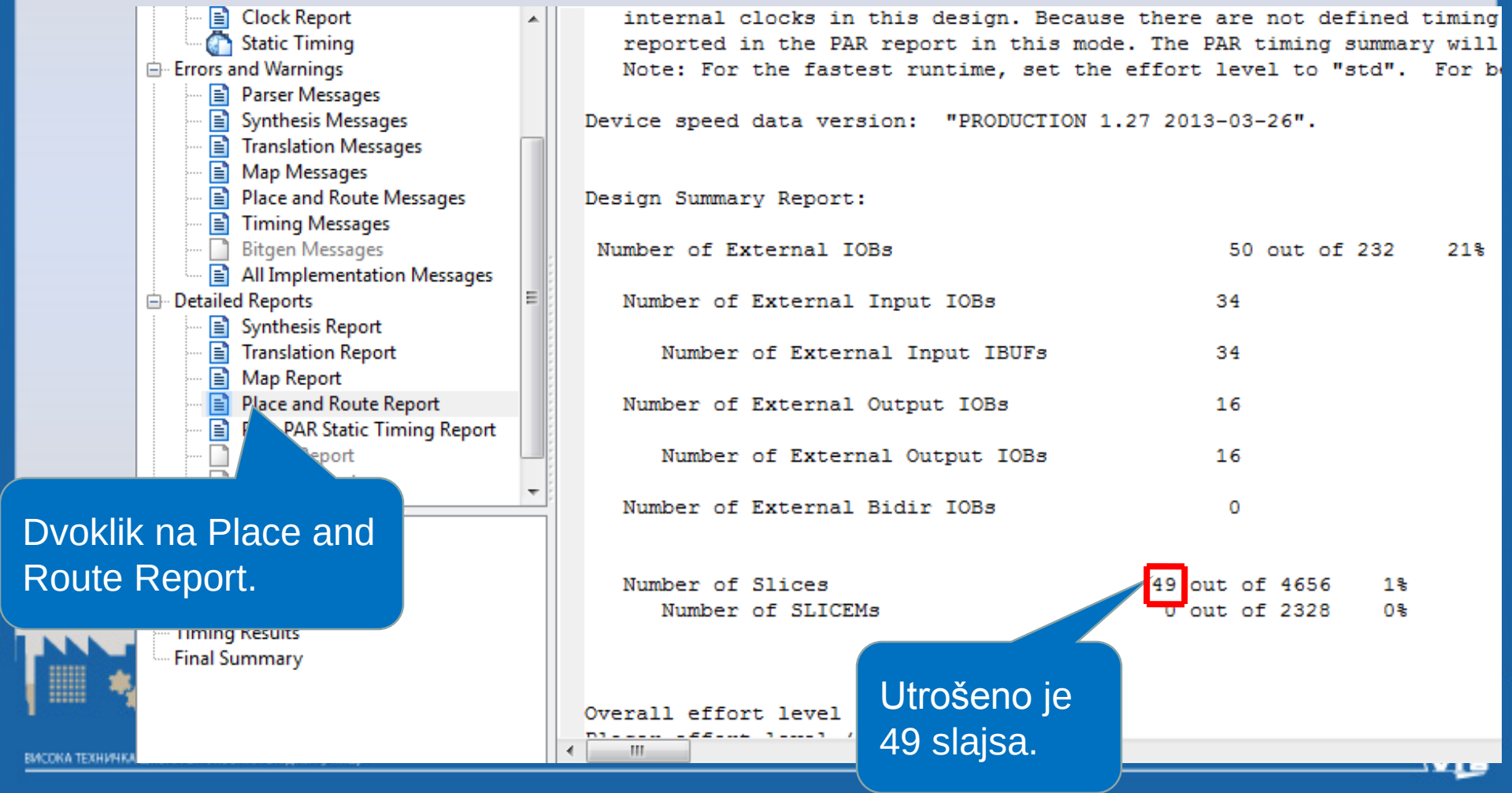




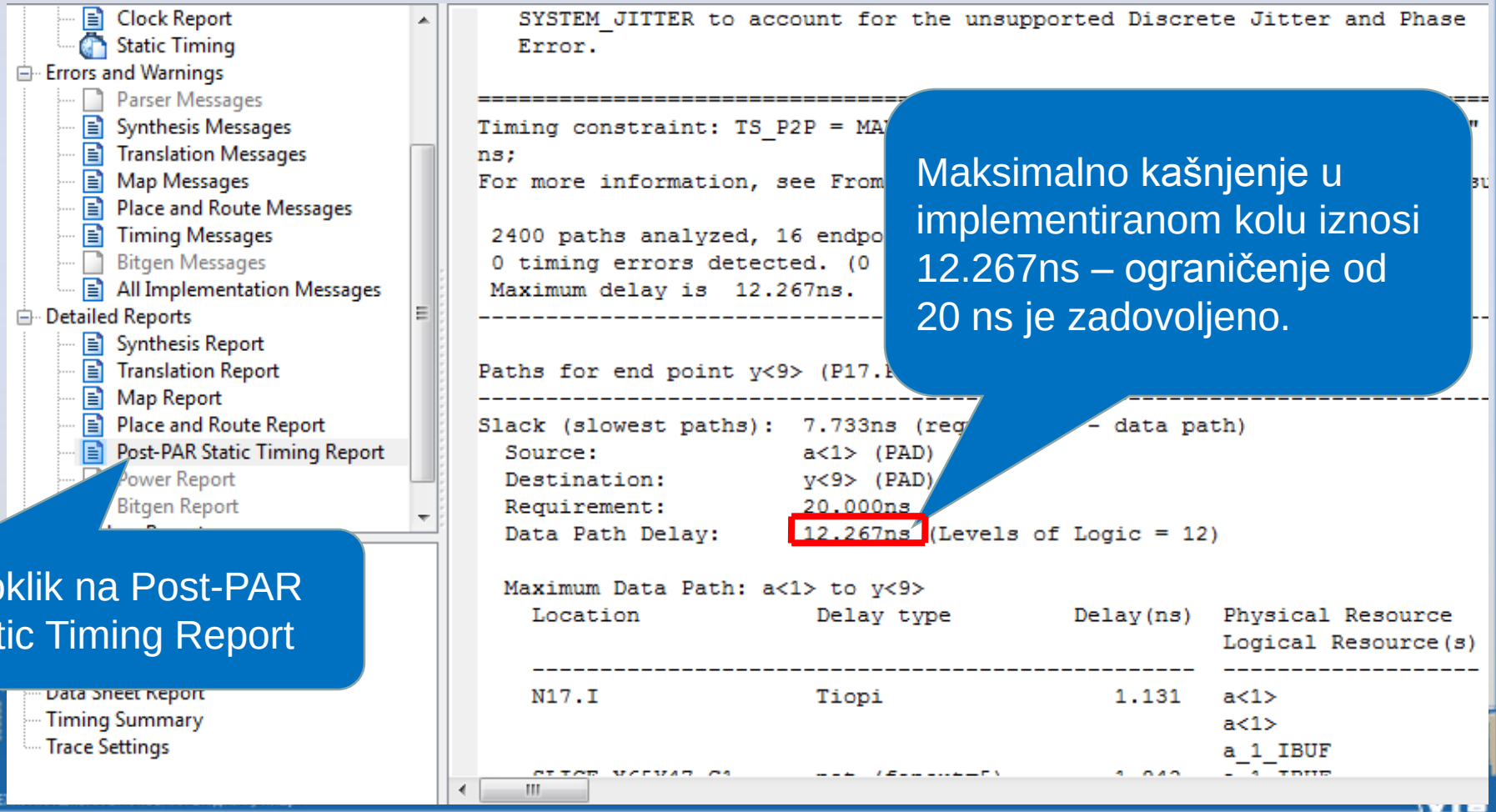


Procena je da kašnjenje kroz logiku (kroz LUT-ove) iznosi 7, 914 ns, a kašnjenje kroz veze 2.504 ns).

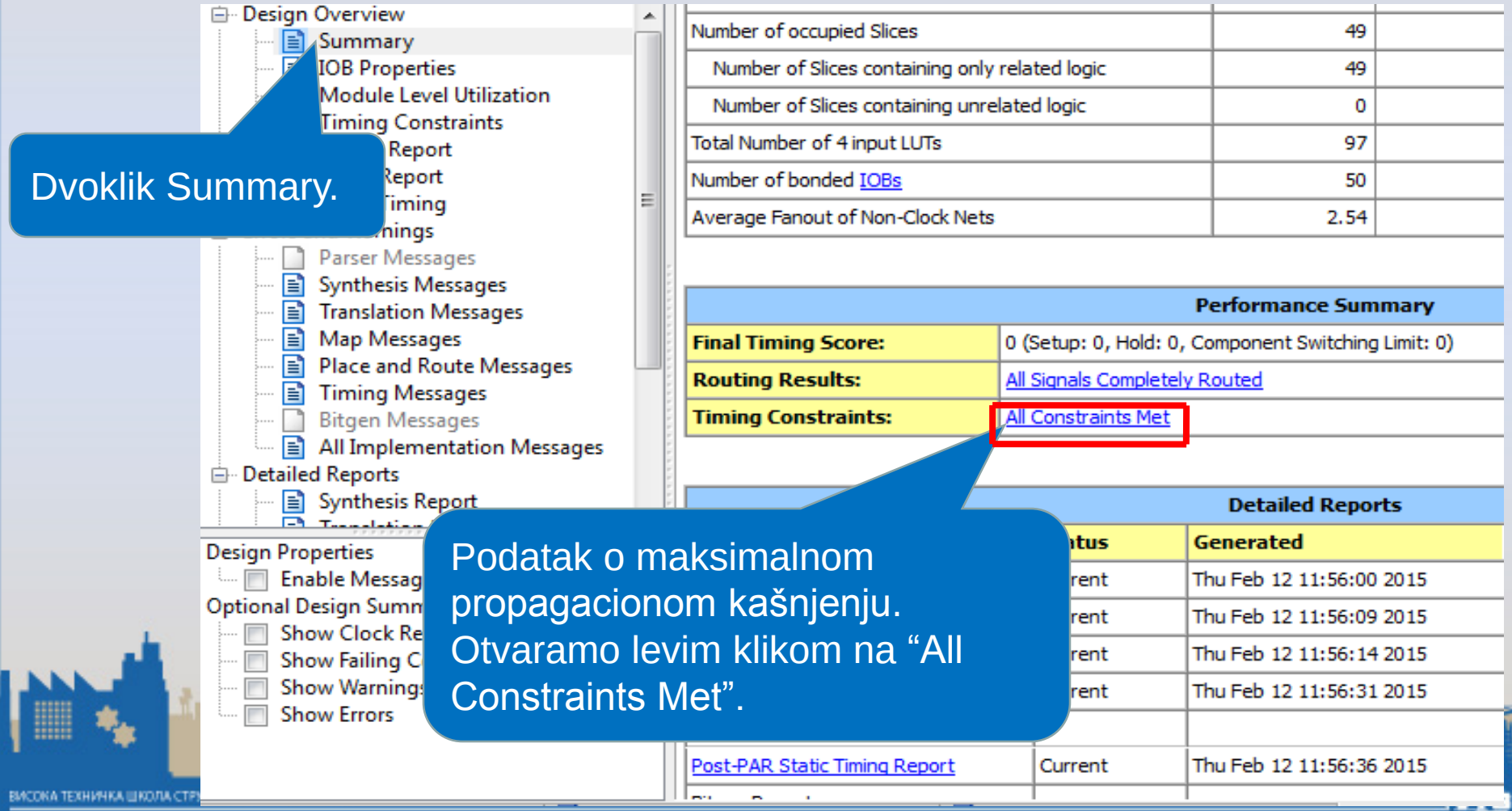
Izveštaj o implementaciji – neoptimizovan kod



Izveštaj o implementaciji – neoptimizovan kod

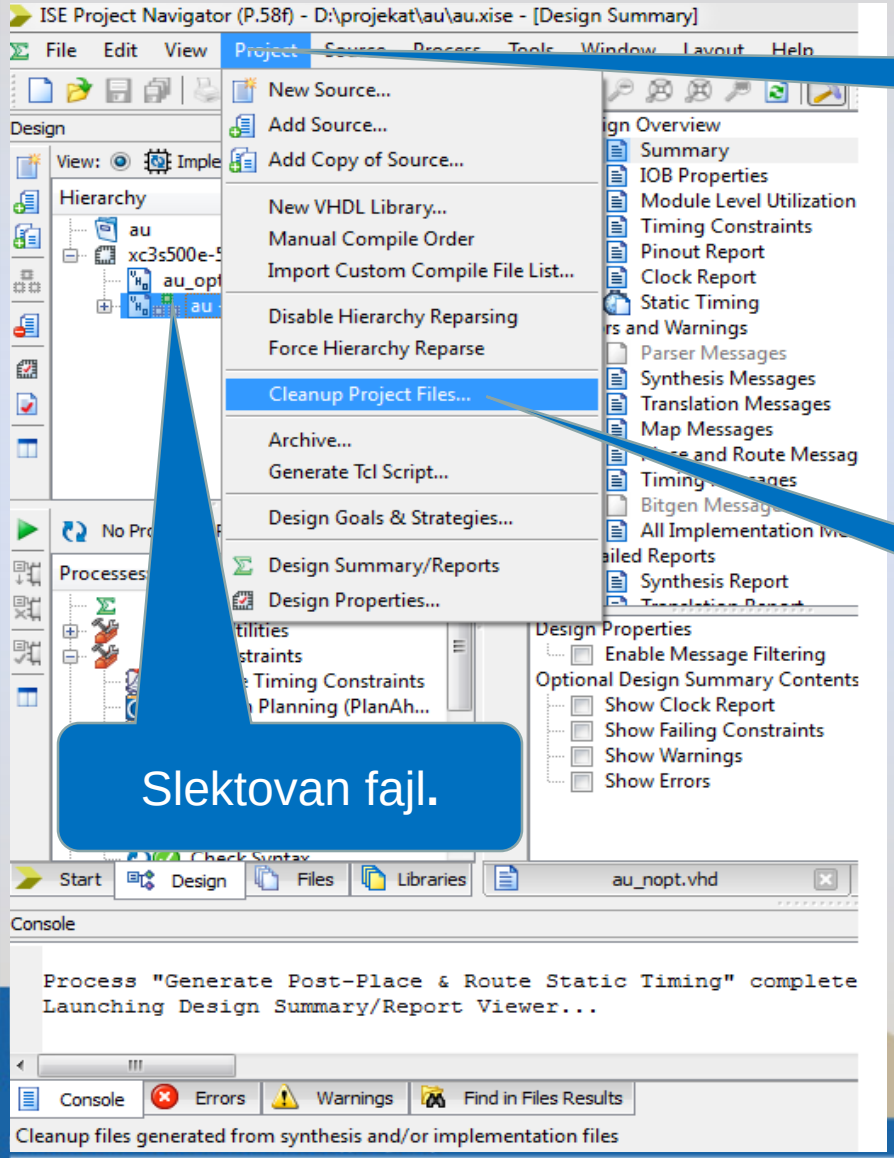


“Design Summary” – neoptimiozvan kod



Podatak o maksimalnom propagacionom kašnjenju

“Čišćenje” projektnog fajla – neoptimizovan kod

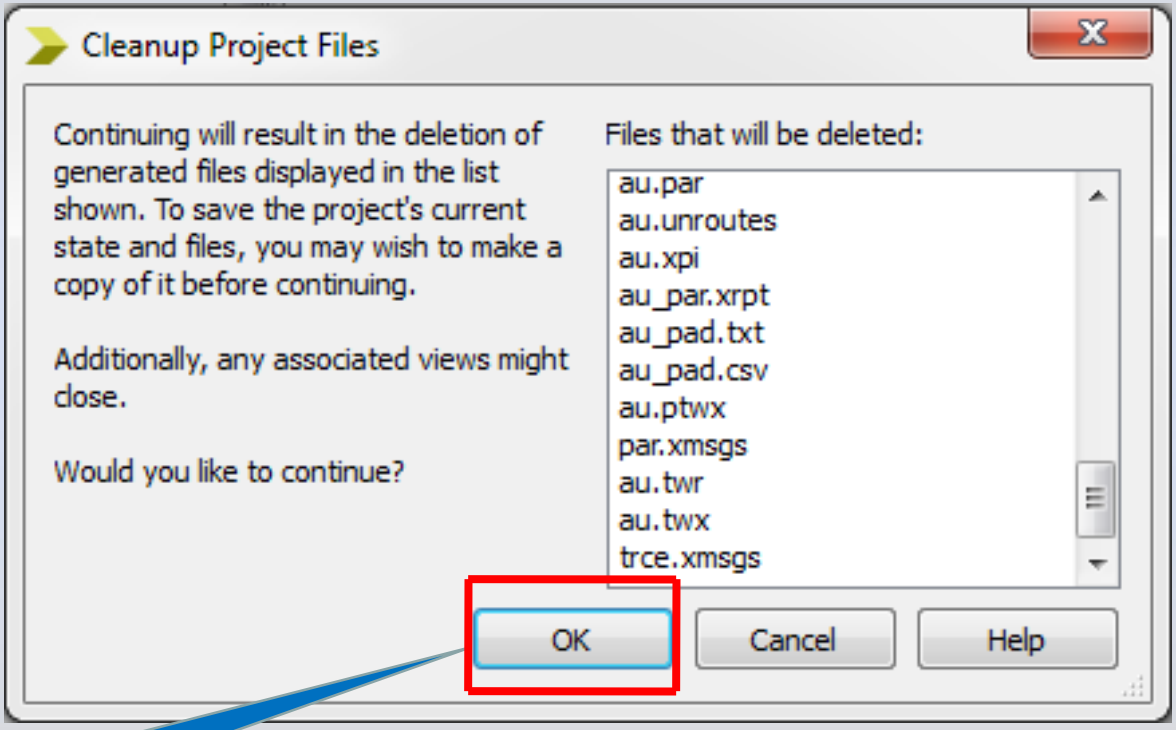


Biramo karticu “Project”.

Obrisati Projektni fajl (Cleanup Project Files).

Slektovan fajl.

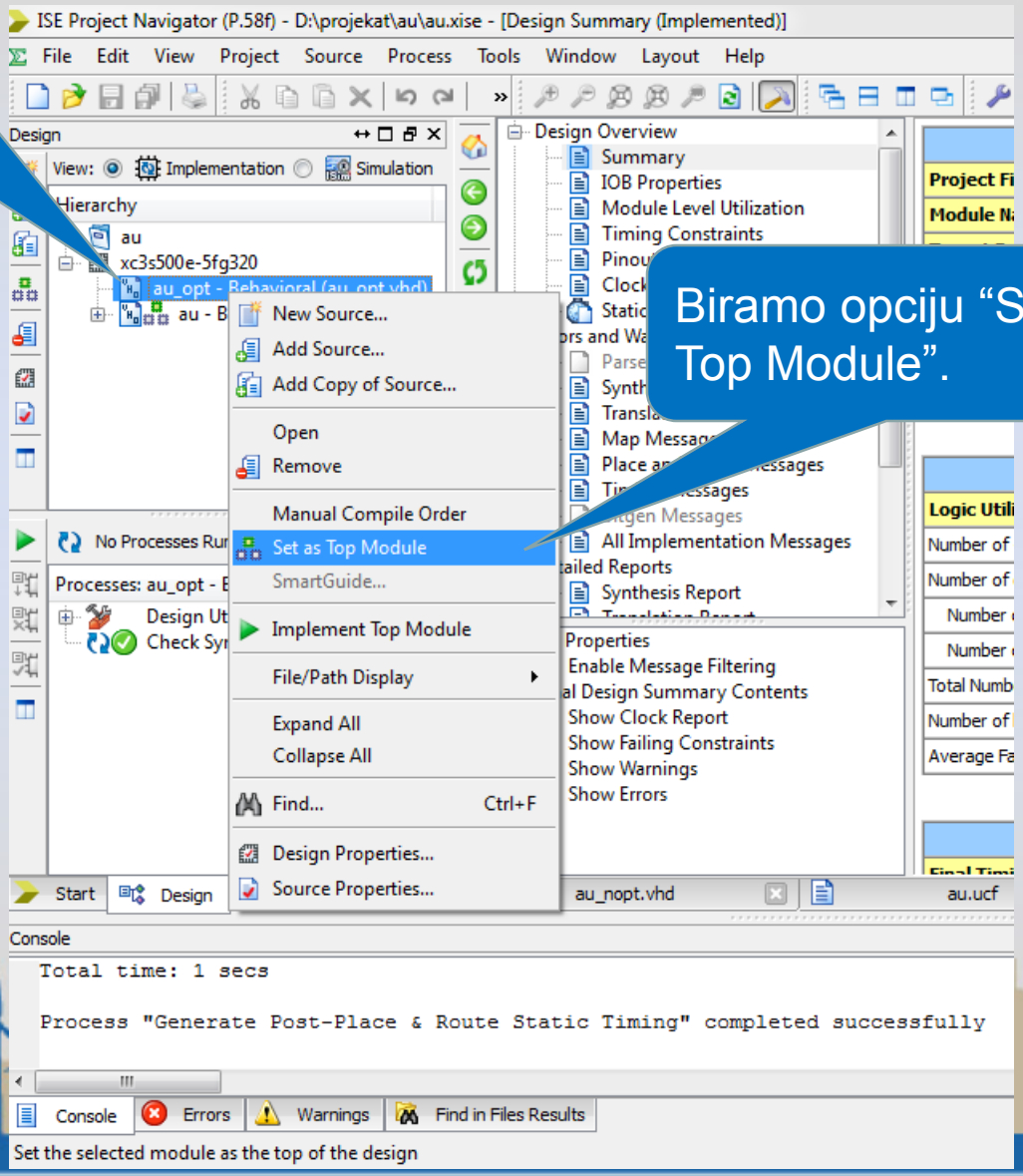
“Čišćenje” projektnog fajla – neoptimizovan kod



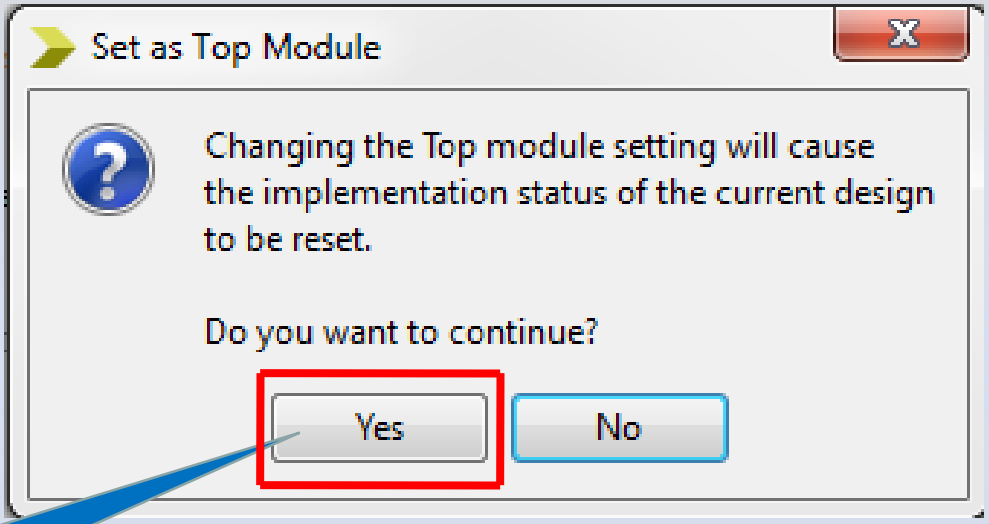
Biramo OK.

Prelazak na optimizovanu arhitekturu

Selektovan je projektni fajl. Desnim klikom na slektovani fajl otvaramo novi prozor.

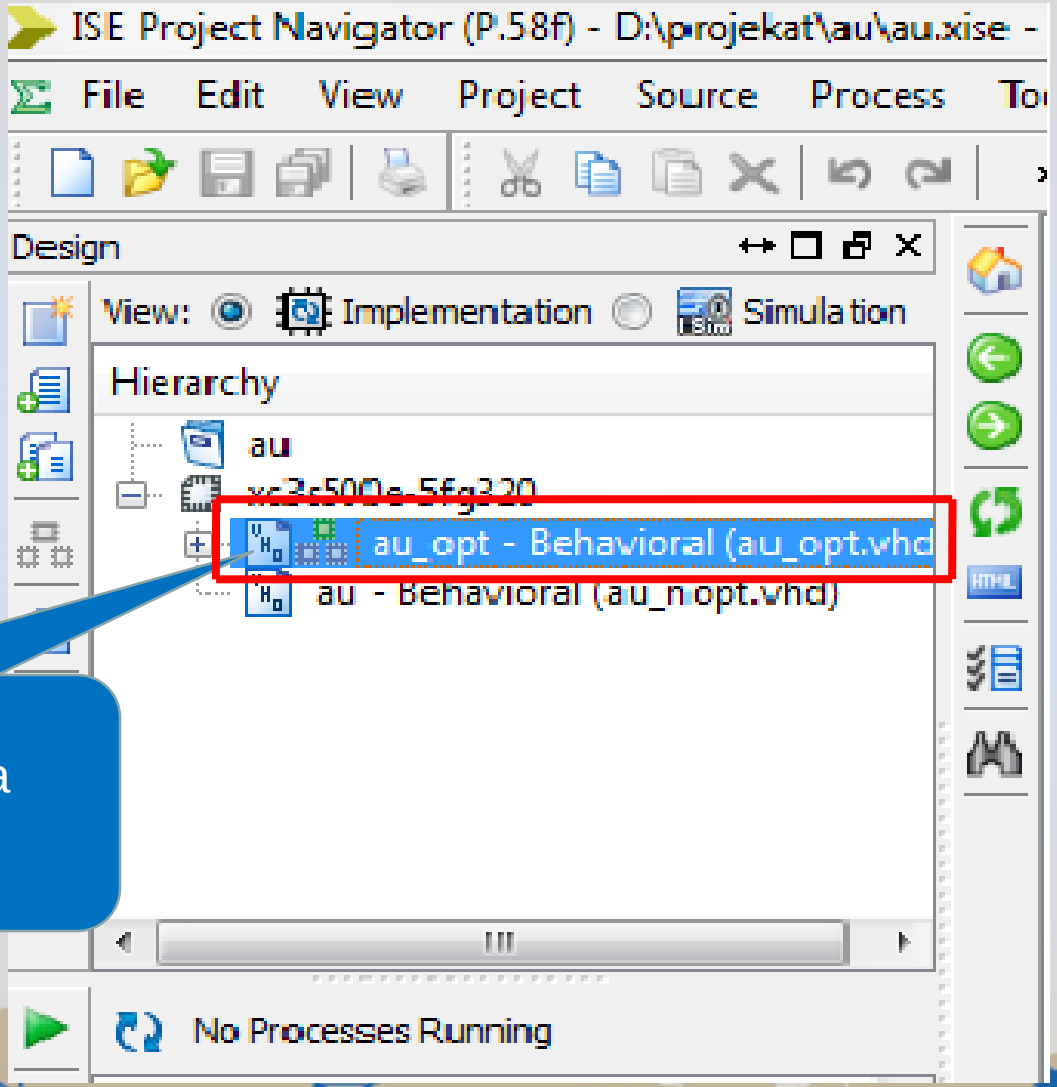


Prelazak na optimizovanu arhitekturu



Biramo YES.

Prelazak na optimizovanu arhitekturu



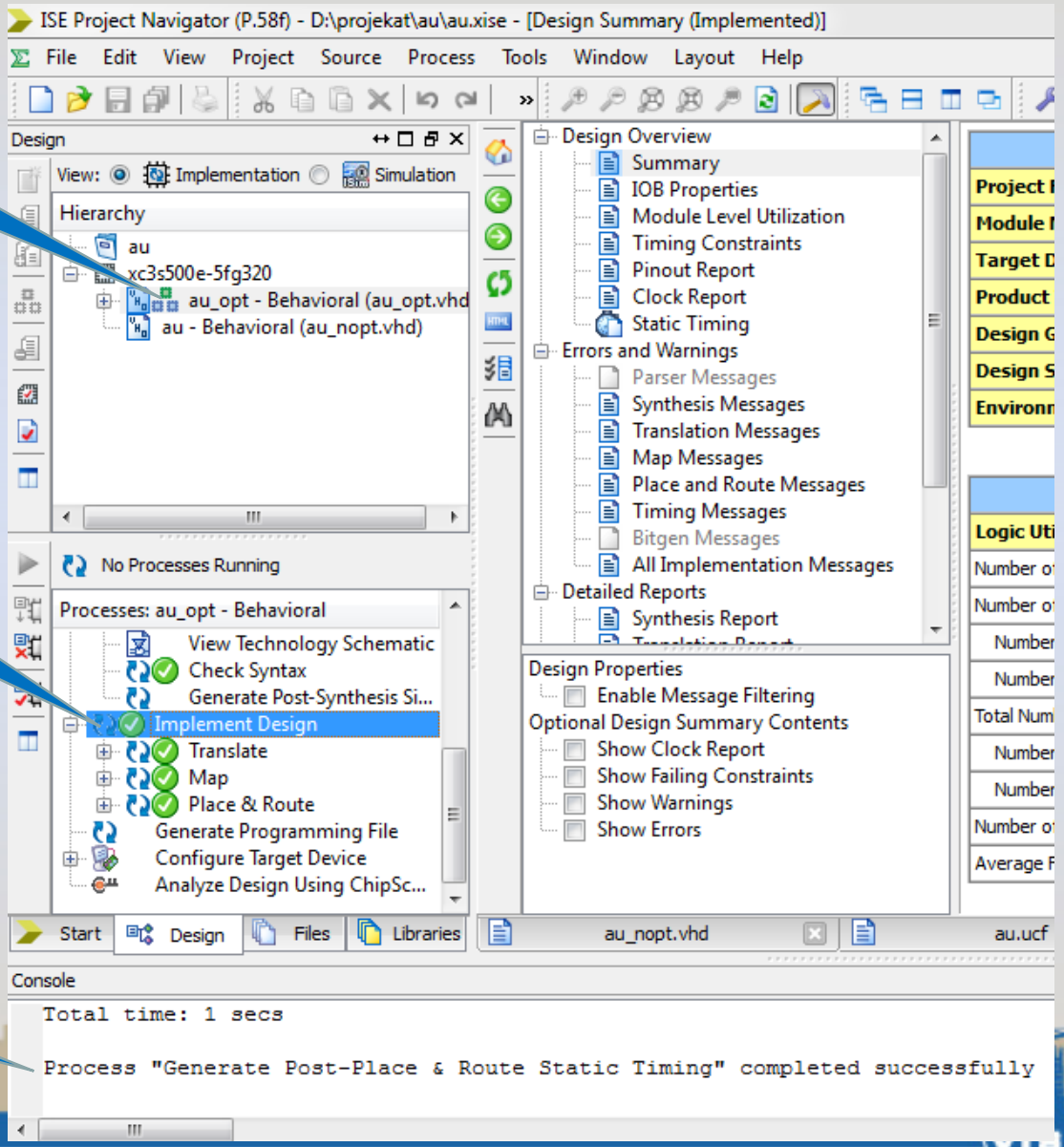
Promenili smo top model na optmizovanu arhitekturu.

Implementacija

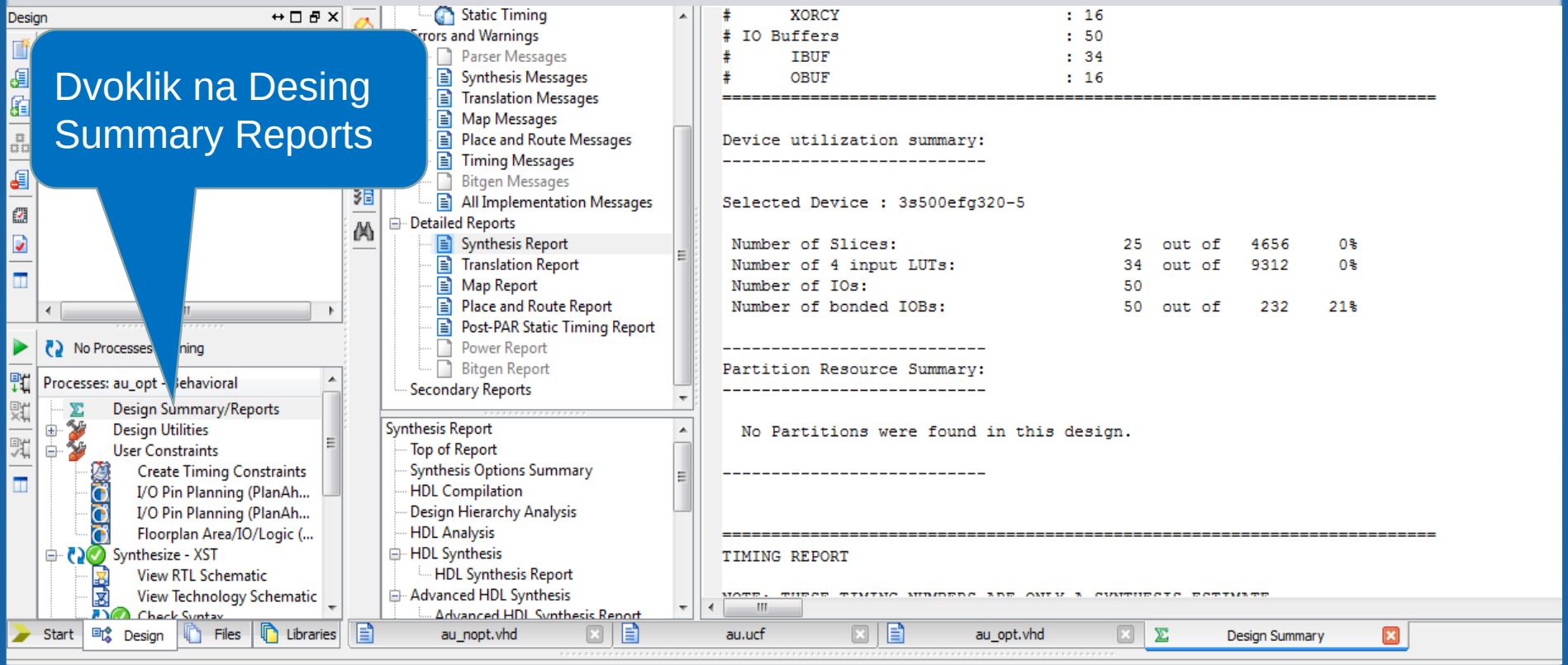
Selektovan je projektni fajl.

Dvoklik na Implement Desing.

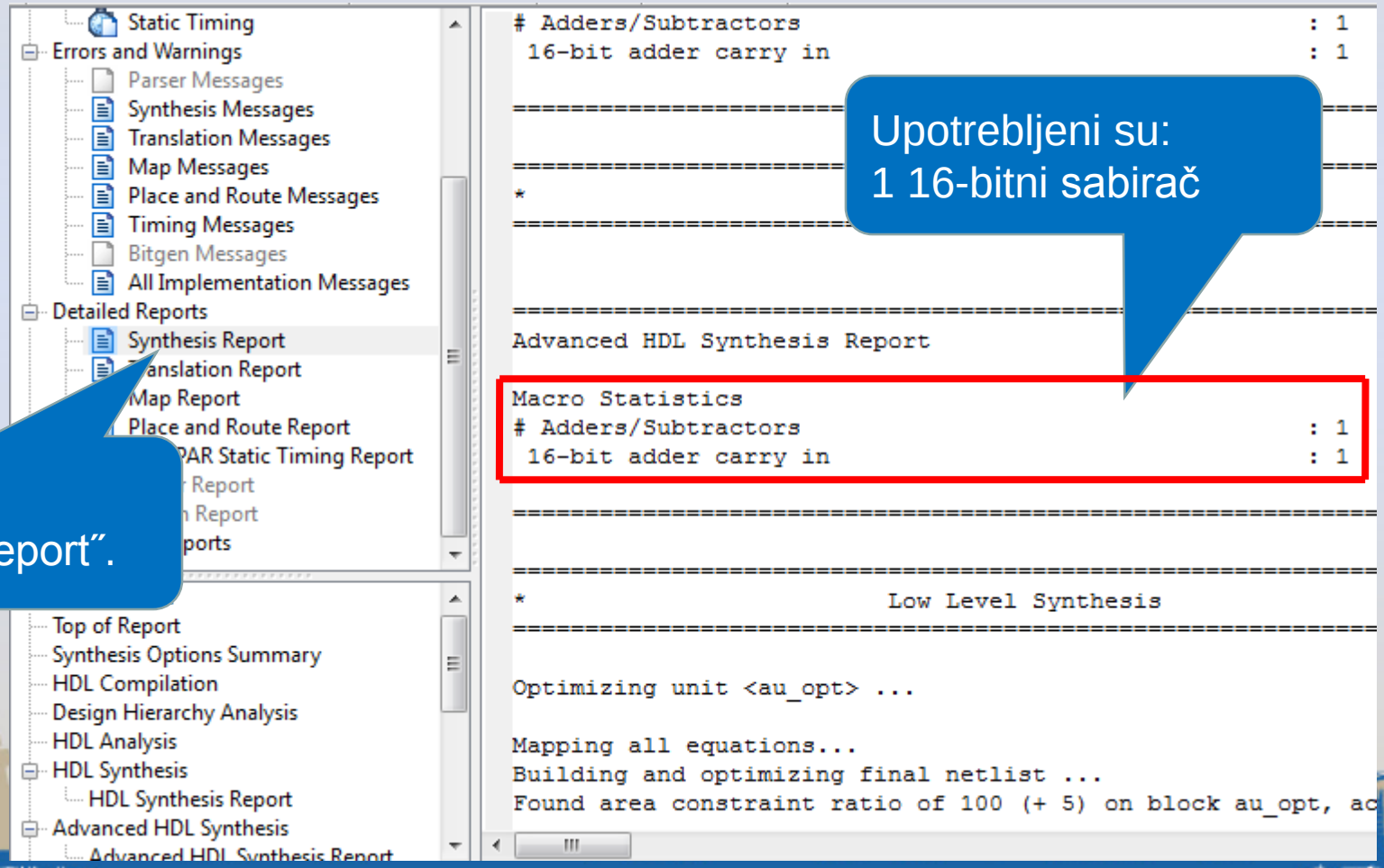
Poruka da je implementacija uspešno okončana.



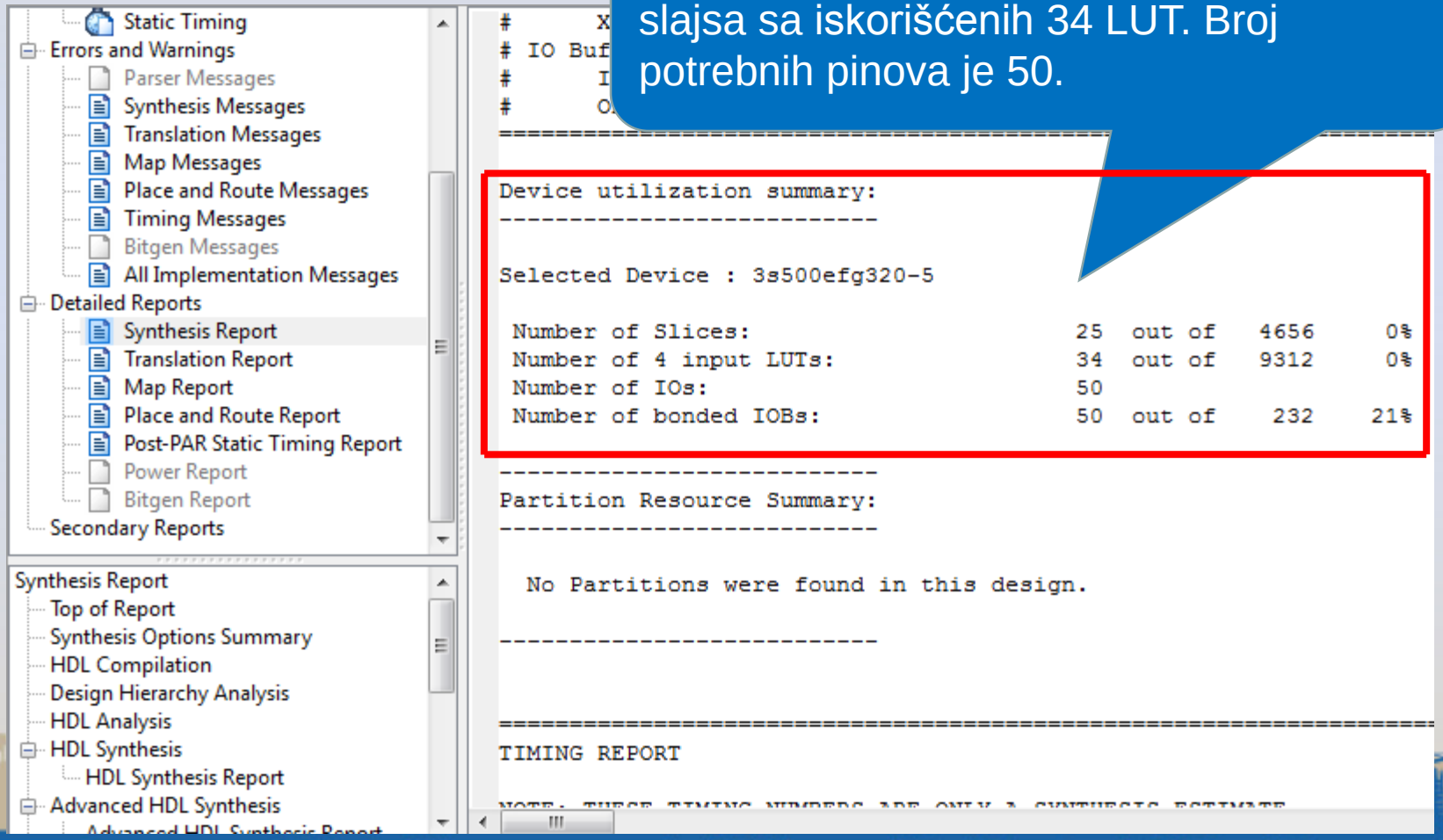
Izveštaj o sintezi – optimizovan kod



Izveštaj o sintezi - optimizovan

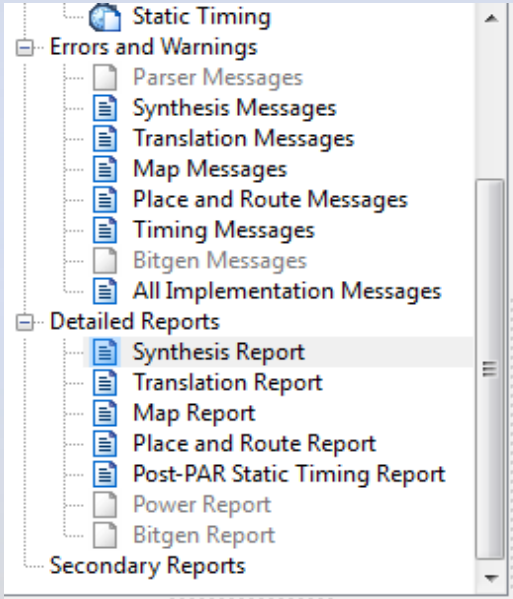


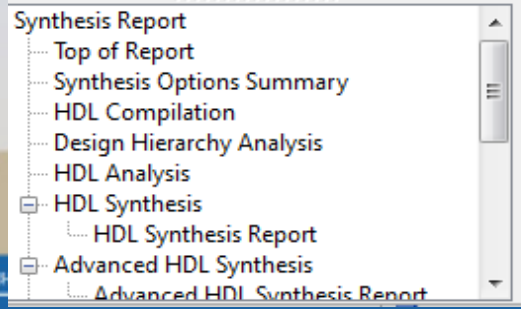
Izveštaj o sintezi – optimizovan kod



Izveštaj o sintezi – optimizovan kod

Maksimalno propagaciono kašnjenje iznosi 10.097 ns i odgovara kašnjenju signala od ulaza b(0) do izlaza y(14). Na toj putanju se nalazi 21 nivoa logike – 21 redno povezanih LUT-ova).

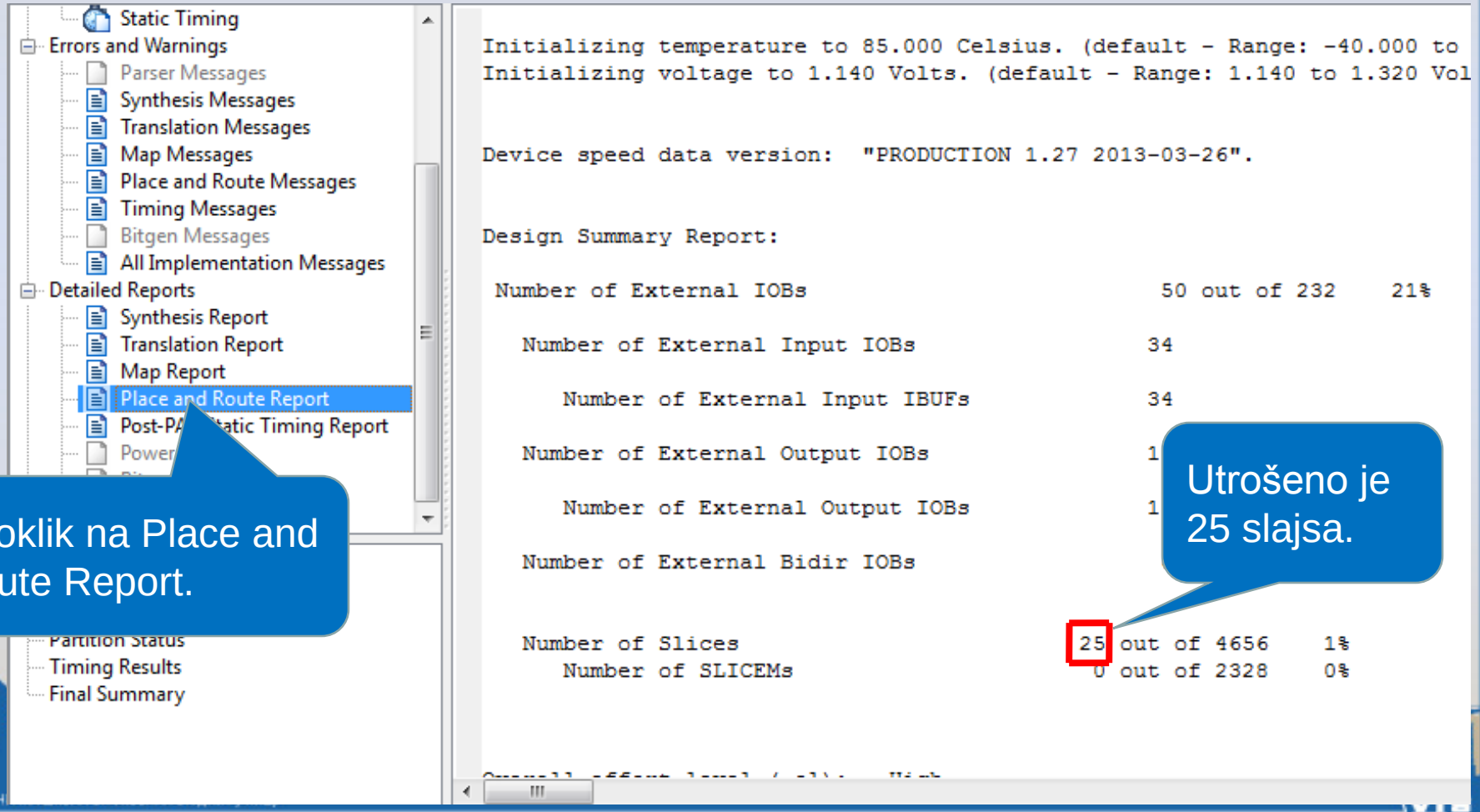




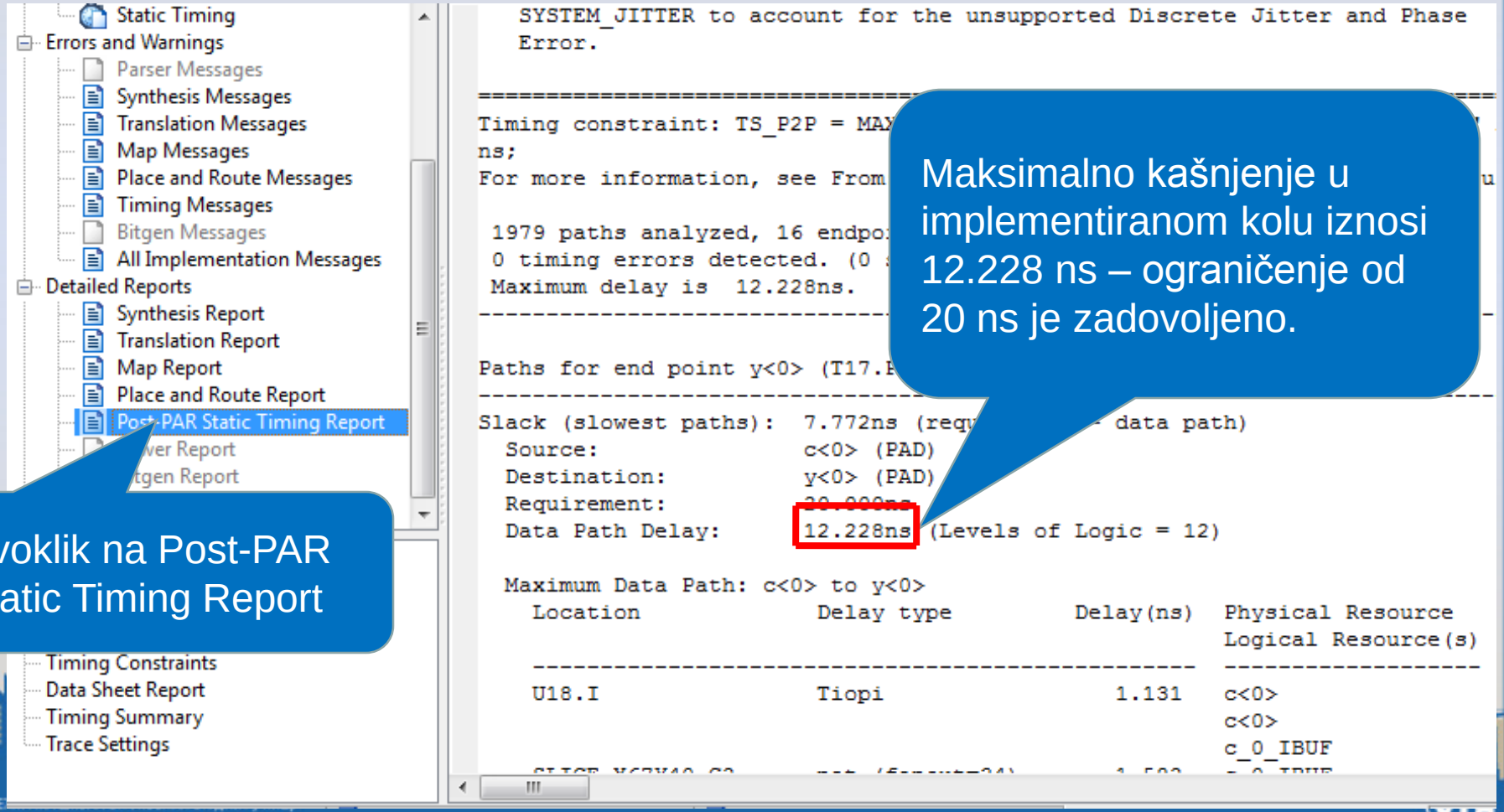

```
Delay:               10.097ns (Levels of Logic = 21)
  Source:            c<0> (PAD)
  Destination:       y<14> (PAD)

  Data Path: c<0> to y<14>
                                        Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             34   1.106   1.225  c_0_IBUF (c_0_IBUF)
     LUT2:I0->O             1   0.612   0.357  cu1 (cu)
     MUXCY:CI->O            1   0.051   0.000  Madd_s_cy<0> (Madd_s_cy<0>)
     MUXCY:CI->O            1   0.051   0.000  Madd_s_cy<1> (Madd_s_cy<1>)
     MUXCY:CI->O            1   0.051   0.000  Madd_s_cy<2> (Madd_s_cy<2>)
     MUXCY:CI->O            1   0.051   0.000  Madd_s_cy<3> (Madd_s_cy<3>)
     MUXCY:CI->O            1   0.051   0.000  Madd_s_cy<4> (Madd_s_cy<4>)
     MUXCY:CI->O            1   0.051   0.000  Madd_s_cy<5> (Madd_s_cy<5>)
     MUXCY:CI->O            1   0.051   0.000  Madd_s_cy<6> (Madd_s_cy<6>)
     MUXCY:CI->O            1   0.051   0.000  Madd_s_cy<7> (Madd_s_cy<7>)
     MUXCY:CI->O            1   0.051   0.000  Madd_s_cy<8> (Madd_s_cy<8>)
     MUXCY:CI->O
     MUXCY:CI->O
     MUXCY:CI->O
     MUXCY:CI->O
     MUXCY:CI->O
     MUXCY:CI->O
     XORCY:CI->O
     LUT4:I2->O
     MUXF5:I1->O
     OBUF:I->O                 3.169          y_9_OBUF
    ----------------------------------------
    Total                     10.097ns (7.249ns logic, 2.848ns route)
                                       (71.8% logic, 28.2% route)
```

Procena je da kašnjenje kroz logiku (kroz LUT-ove) iznosi 7, 249 ns, a kašnjenje kroz veze 2.848 ns).

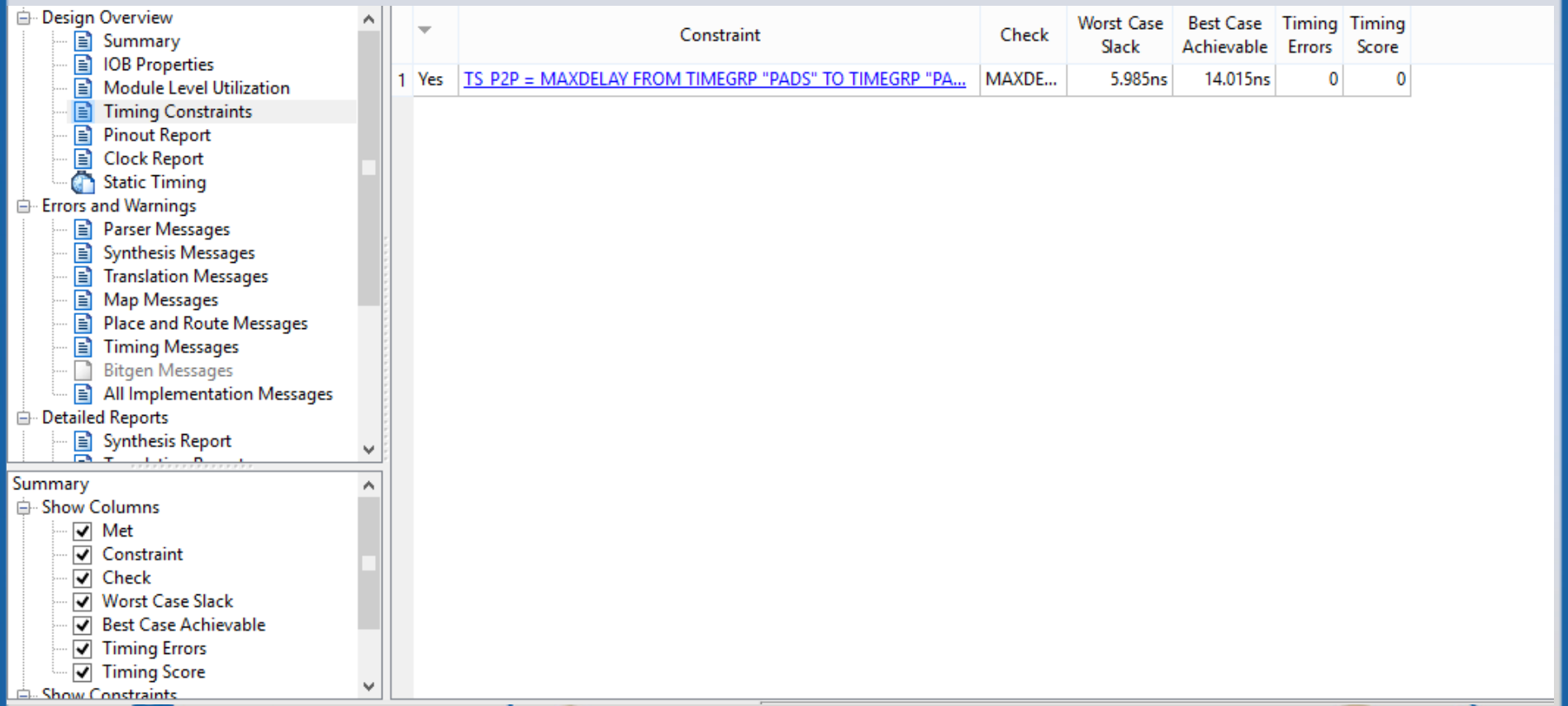
Izveštaj o implementaciji – optimizovan kod



Izveštaj o implementaciji – optimizovan kod



Podatak o maksimalnom propagacionom kašnjenju



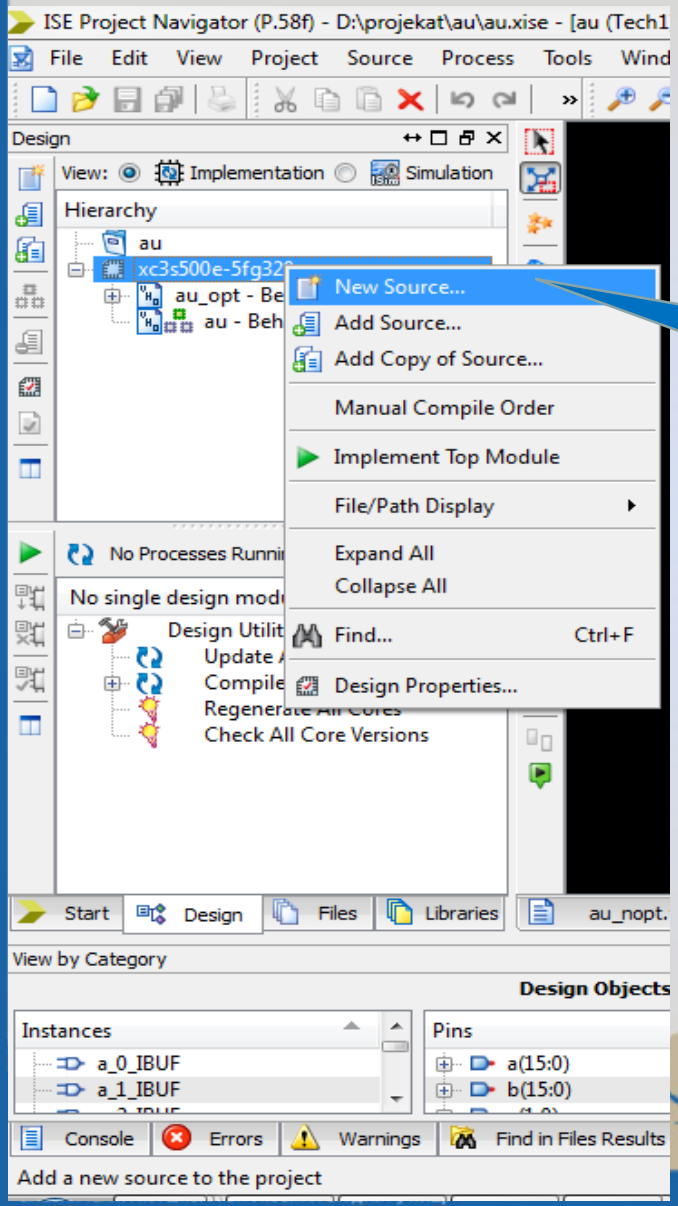
Rezultati sinteze i implementacije neoptimizovane AU

Podaci o implementaciji		
RTL komponente 1 sabirač 1 oduzimač 1 komparator za veće 1 komparator za manje 1 multiplekser 4-u-1		
Podaci o implementaciji		
N (broj bitova)	Slice (broj potrošenih slajsova)	Tp [ns] (max. prop. kašnjenja)
4	11	10.651 ns
8	25	10.298 ns
16	49	12.267 ns

Rezultati sinteze i implementacije optimizovane AU

Podaci o implementaciji		
RTL komponente 1 sabirač/oduzimač		
Podaci o implementaciji		
N (broj bitova)	Slice (broj potrošenih slajsova)	Tp [ns] (max. prop. kašnjenja)
4	7	10.083 ns
8	13	10.759 ns
16	25	12.228 ns

Generisanje testbenča



Desnim klikom preko imenaVHDL modula, a onda New Source.

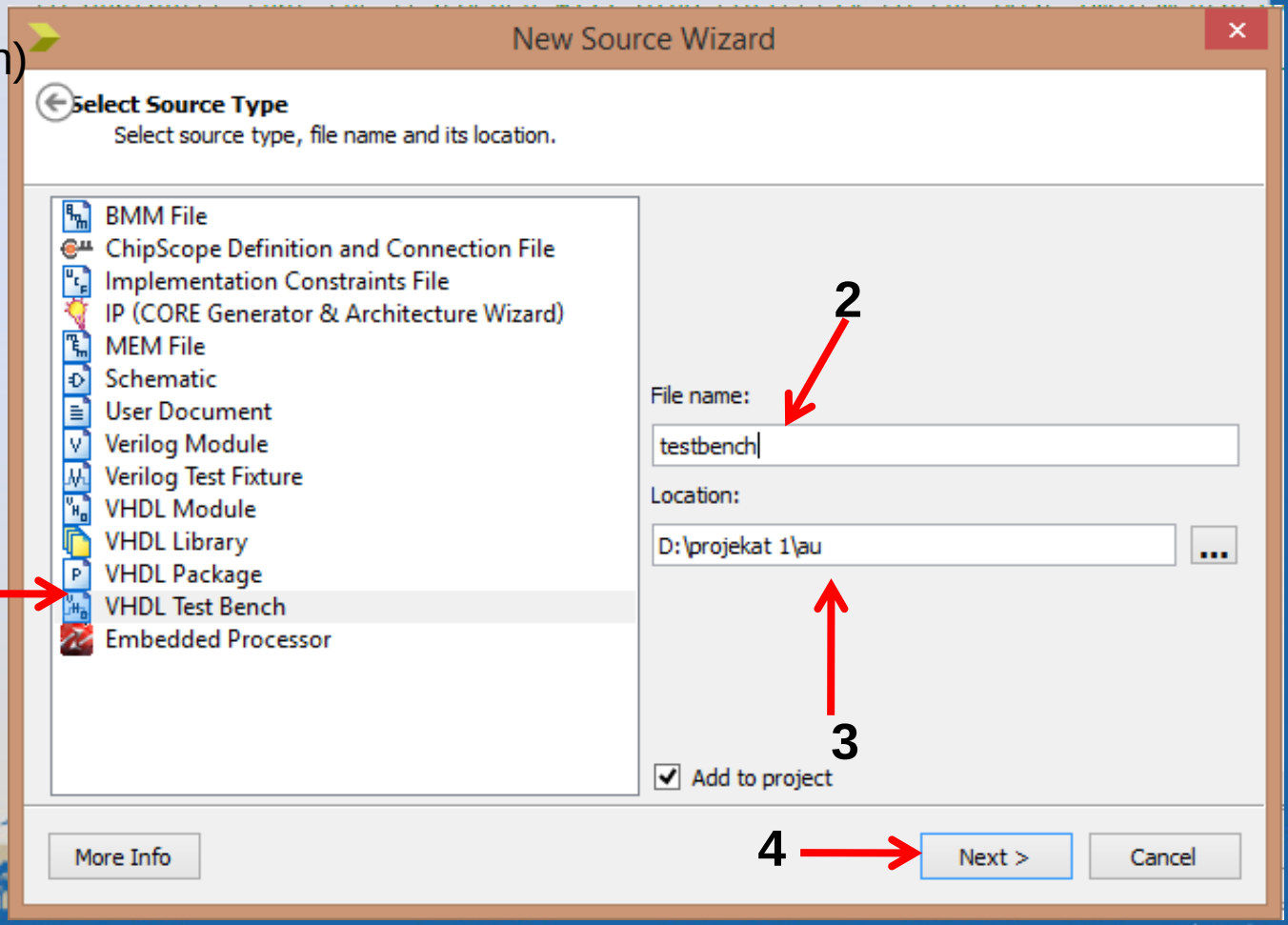
Generisanje testbenča

1.Izbor tipa projektnog fajla (biramo VHDL Test Bench)

2.Upišite ime projektnog fajla (neka bude testbench)

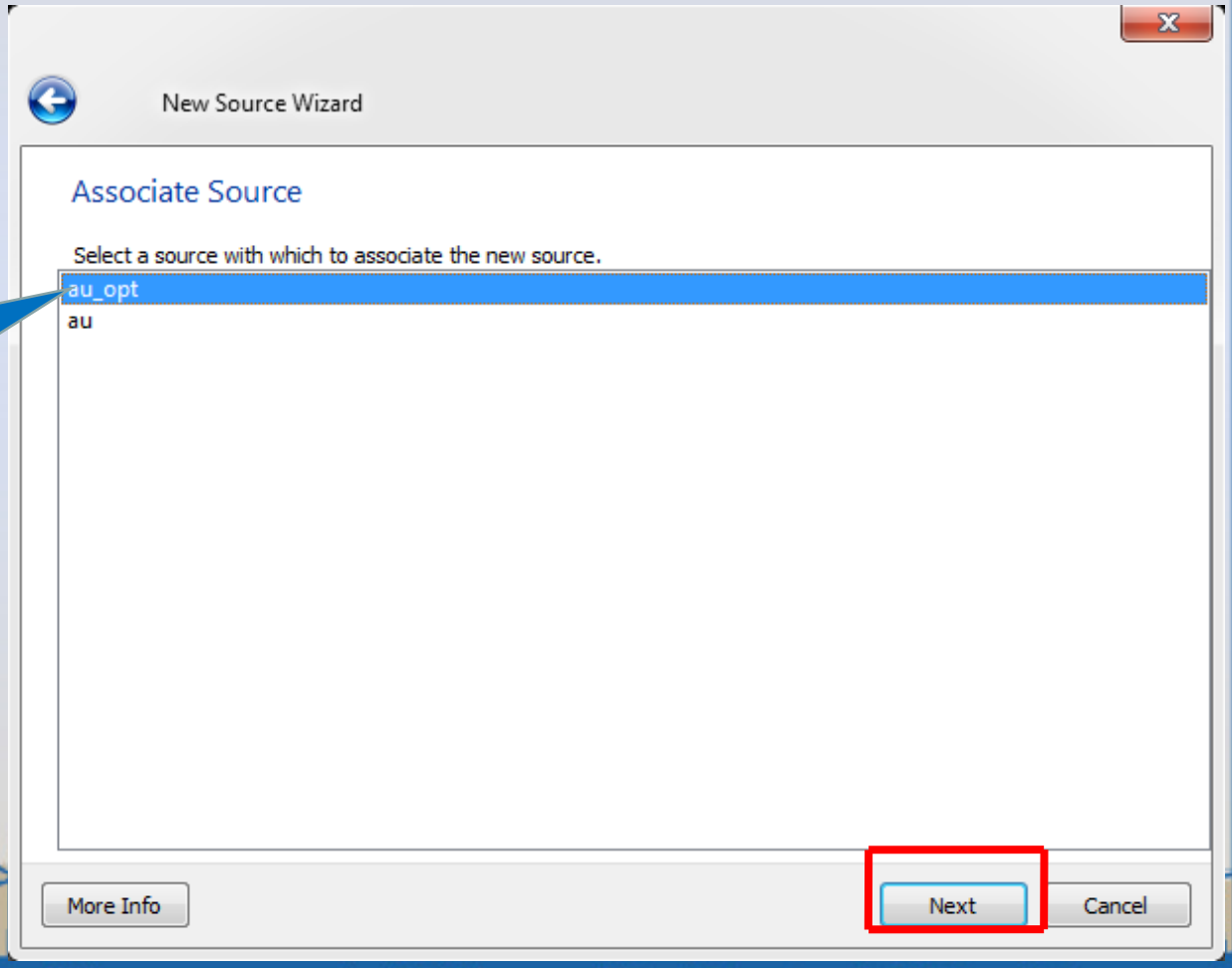
3.Lokacija -neka ostane predložena lokacija

4.Next

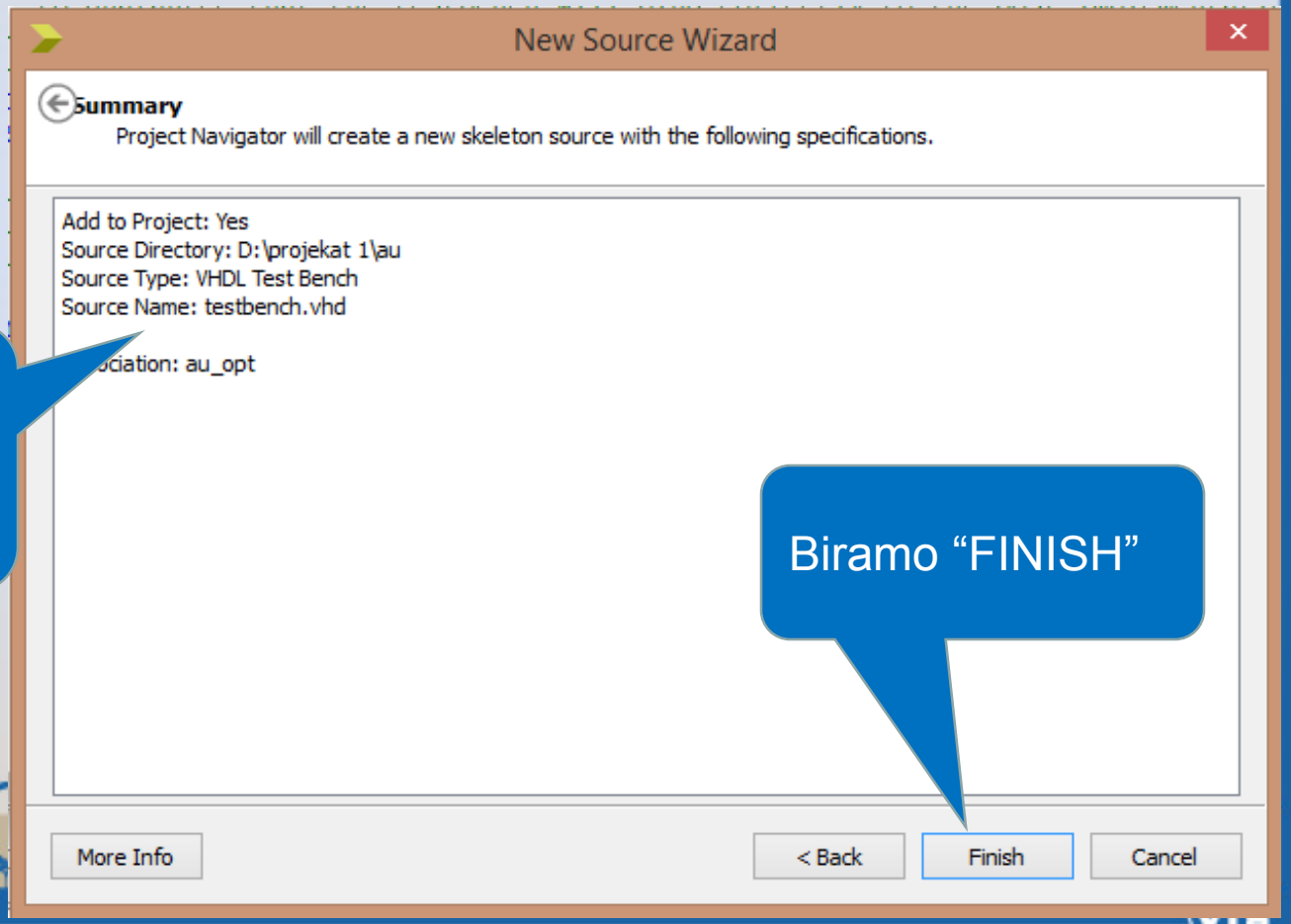


Generisanje testbenča

Mi biramo VHDL Modul “au_opt”, pa biramo opciju “Next”.



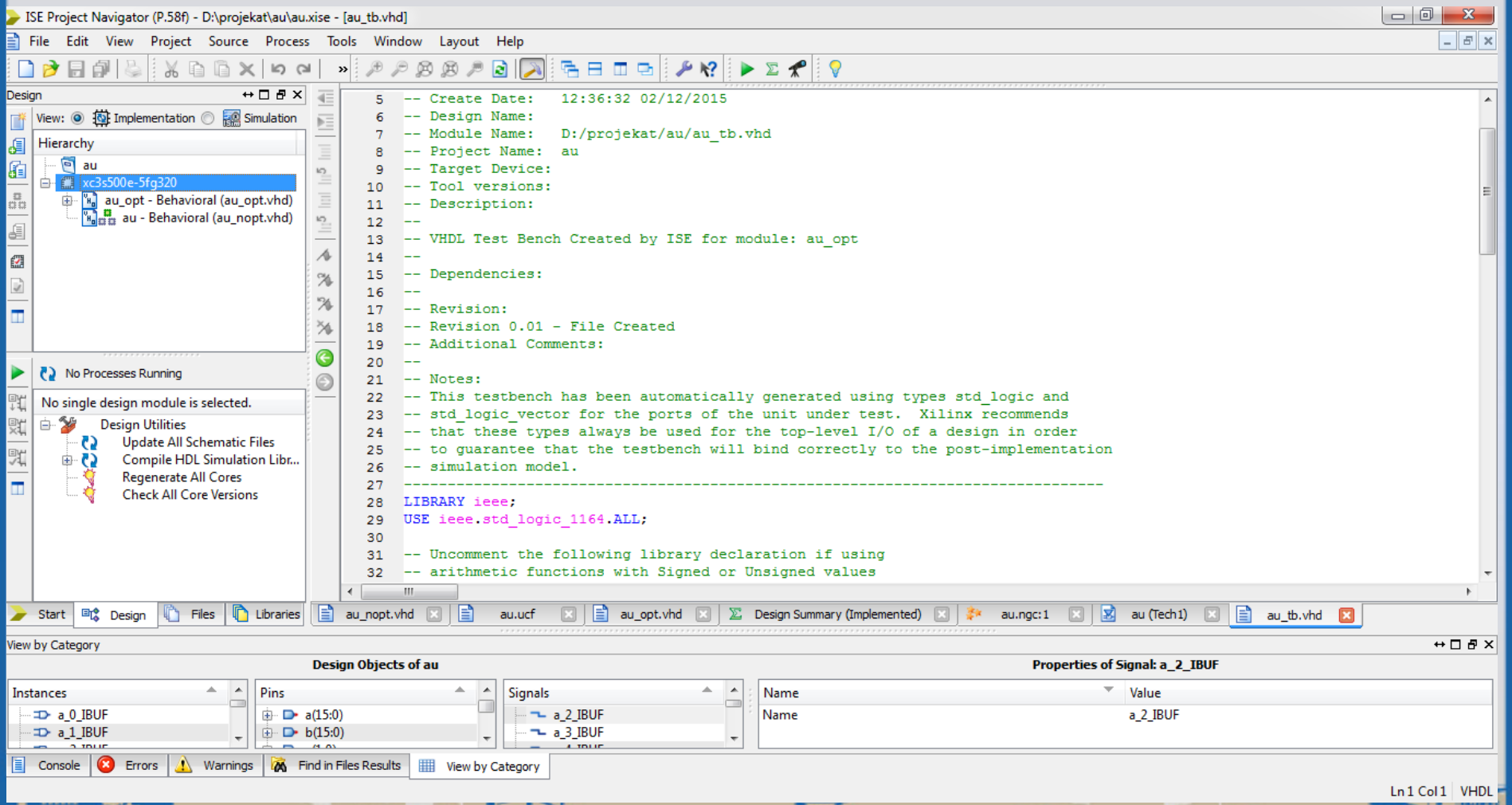
Rezime testbenča



Informativni dijalog o testbenču

Biramo “FINISH”

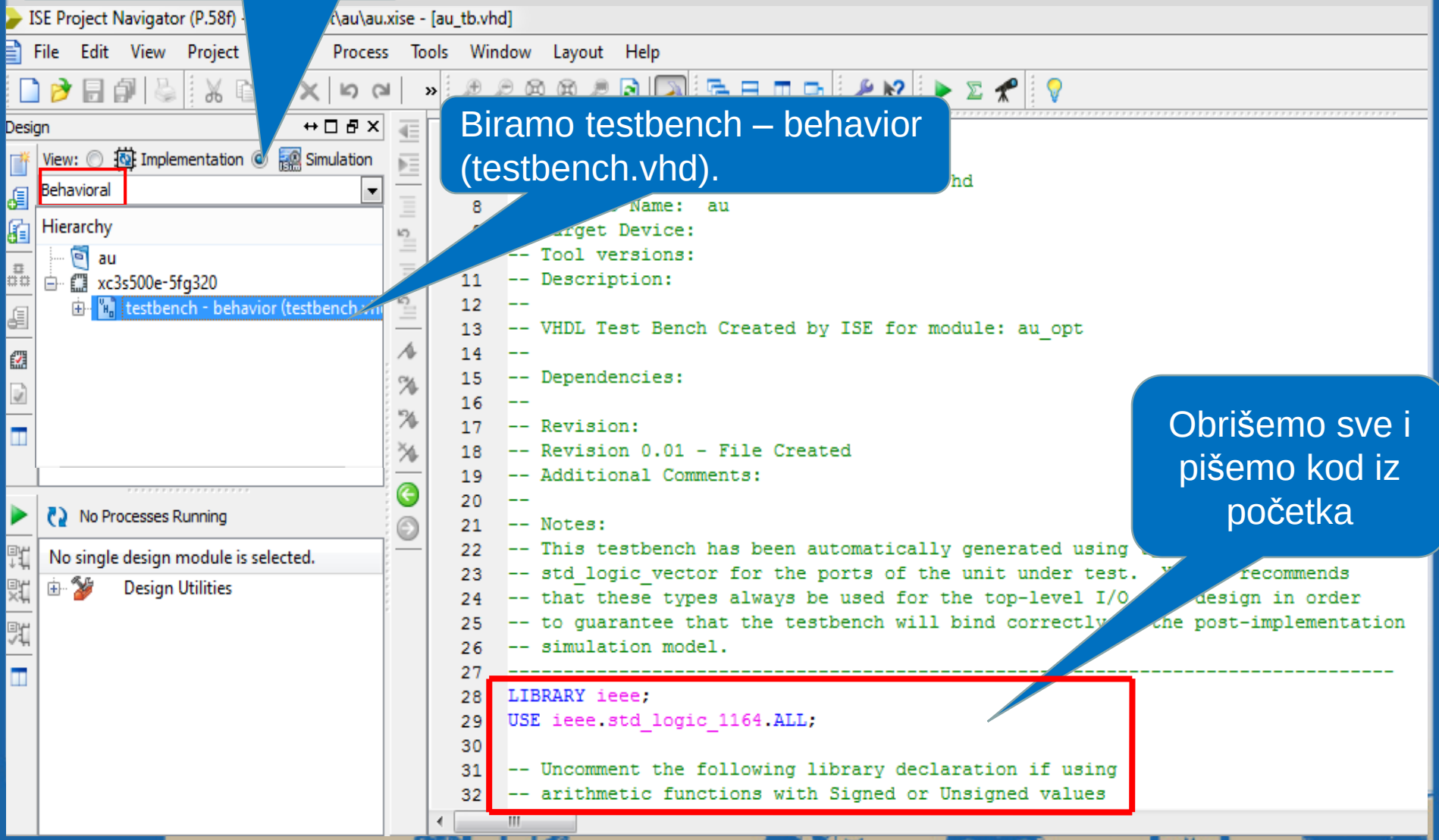
Testbenč


ISE Project Navigator (P.58f) - D:\projekat\au\au.xise - [au_tb.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
au
xc3s500e-5fg320
au_opt - Behavioral (au_opt.vhd)
au - Behavioral (au_nopt.vhd)
No Processes Running
No single design module is selected.
Design Utilities
Update All Schematic Files
Compile HDL Simulation Libr...
Regenerate All Cores
Check All Core Versions
5 -- Create Date: 12:36:32 02/12/2015
6 -- Design Name:
7 -- Module Name: D:/projekat/au/au_tb.vhd
8 -- Project Name: au
9 -- Target Device:
10 -- Tool versions:
11 -- Description:
12 --
13 -- VHDL Test Bench Created by ISE for module: au_opt
14 --
15 -- Dependencies:
16 --
17 -- Revision:
18 -- Revision 0.01 - File Created
19 -- Additional Comments:
20 --
21 -- Notes:
22 -- This testbench has been automatically generated using types std_logic and
23 -- std_logic_vector for the ports of the unit under test. Xilinx recommends
24 -- that these types always be used for the top-level I/O of a design in order
25 -- to guarantee that the testbench will bind correctly to the post-implementation
26 -- simulation model.
27 --
28 LIBRARY ieee;
29 USE ieee.std_logic_1164.ALL;
30
31 -- Uncomment the following library declaration if using
32 -- arithmetic functions with Signed or Unsigned values
Start Design Files Libraries
au_nopt.vhd au.ucf au_opt.vhd Design Summary (Implemented) au.ngc:1 au (Tech1) au_tb.vhd
View by Category
Design Objects of au
Instances
a_0_IBUF
a_1_IBUF
Pins
a(15:0)
b(15:0)
Signals
a_2_IBUF
a_3_IBUF
Properties of Signal: a_2_IBUF
Name
Value
Name
a_2_IBUF
Console Errors Warnings Find in Files Results View by Category
Ln 1 Col 1 VHDL

Testbenč

Biramo Simulation.

Biramo testbench – behavior (testbench.vhd).



Obrišemo sve i pišemo kod iz početka

Testbenč - kod

```
1
2  LIBRARY ieee;
3  USE ieee.std_logic_1164.ALL;
4
5  ENTITY testbench IS
6  END testbench;
7
8  ARCHITECTURE behavior OF testbench IS
9
10     -- Component Declaration for the Unit Under Test (UUT)
11
12     COMPONENT au_opt
13     PORT(
14          a : IN  std_logic_vector(15 downto 0);
15          b : IN  std_logic_vector(15 downto 0);
16          c : IN  std_logic_vector(1 downto 0);
17          y : OUT  std_logic_vector(15 downto 0)
18         );
19     END COMPONENT;
20
21
22    --Inputs
23    signal a : std_logic_vector(15 downto 0) := (others => '0');
24    signal b : std_logic_vector(15 downto 0) := (others => '0');
25    signal c : std_logic_vector(1 downto 0) := (others => '0');
26
27    --Outputs
28    signal y : std_logic_vector(15 downto 0);
29    -- No clocks detected in port list. Replace <clock> below with
30    -- appropriate port name
```

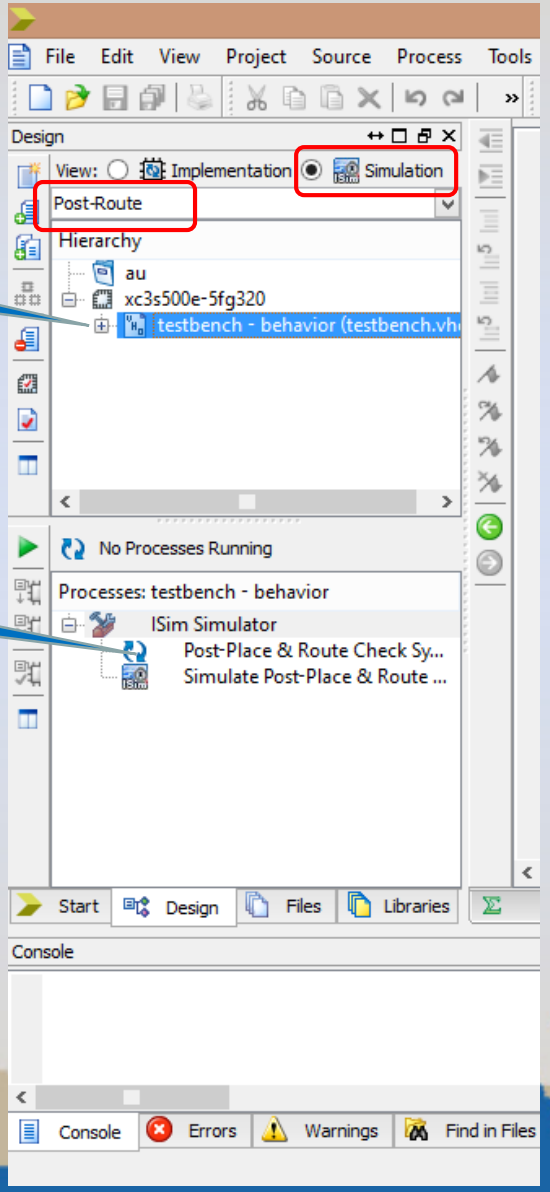
Testbenč - kod

```
35    -- Instantiate the Unit Under Test (UUT)
36    uut: au_opt PORT MAP (
37           a => a,
38           b => b,
39           c => c,
40           y => y
41         );
42
43    -- Stimulus process
44    stim_proc: process
45    begin
46
47       a<="0000000000000001";
48       b<="0000000000001000";
49
50       c<="00";
51       wait for 20 ns;
52
53       a<="0011100000000001";
54       b<="0100000000001100";
55       c<="01";
56       wait for 20 ns;
57       c<="10";
58       wait for 20 ns;
59       c<="11";
60       wait for 20 ns;
61
62    end process;
63
64 END;
```

Provera sintakse i pokretanje simulatora

Selektovanje Testbench-a.

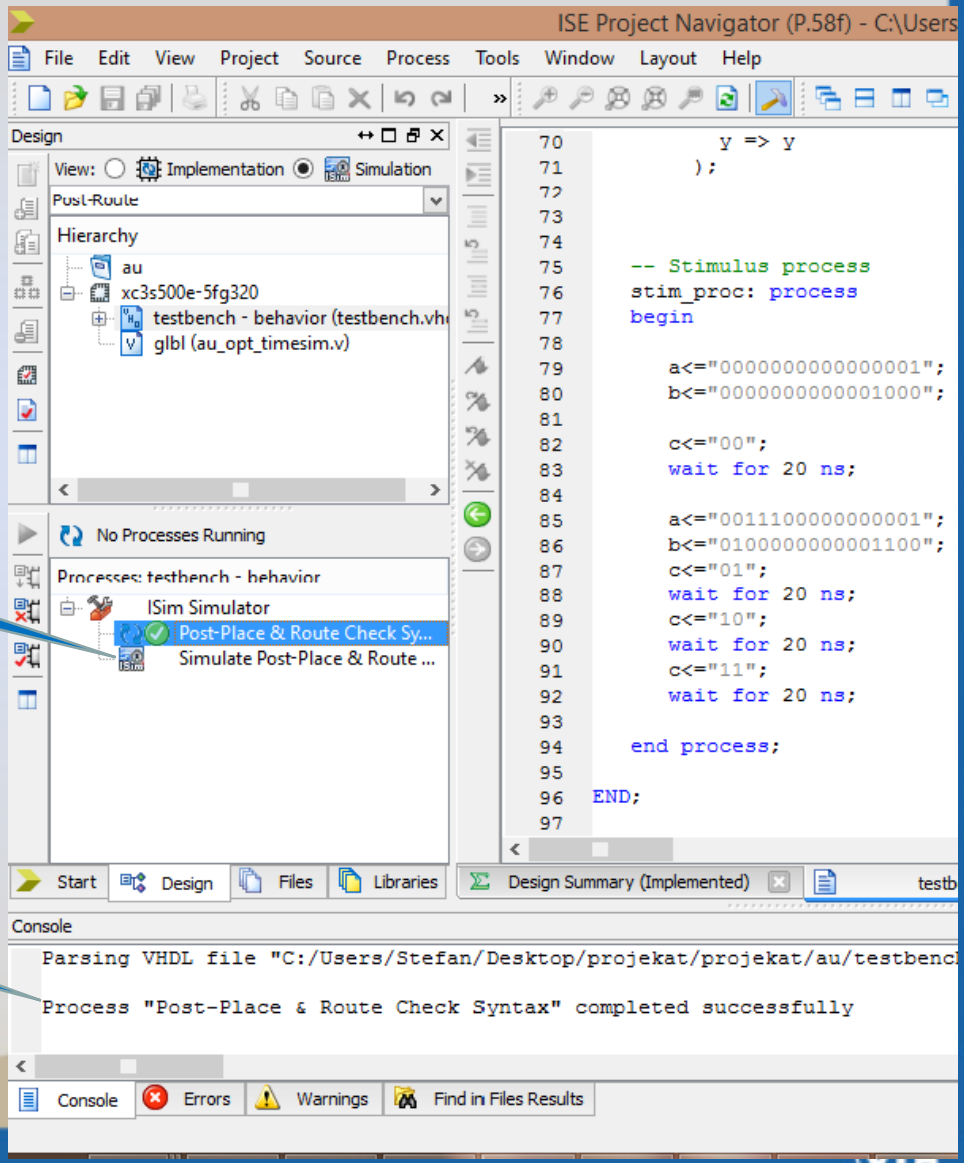
Dvoklik na Post-Place & Route Check Syntax.



Provera sintakse i pokretanje simulatora

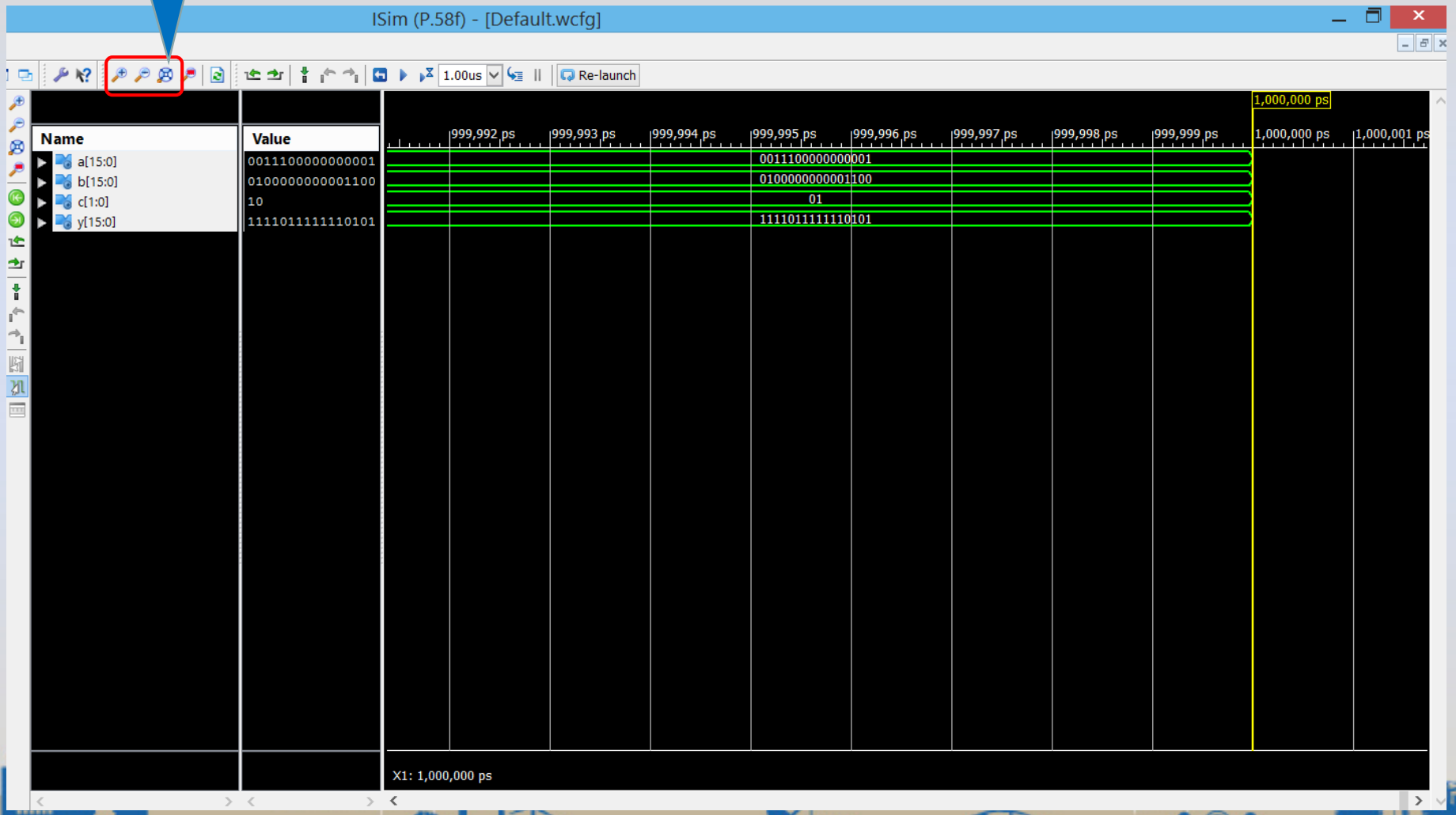
1. Dvoklik na Simulate Behavioral Model.

2. Poruka o ispravnosti sintakse.

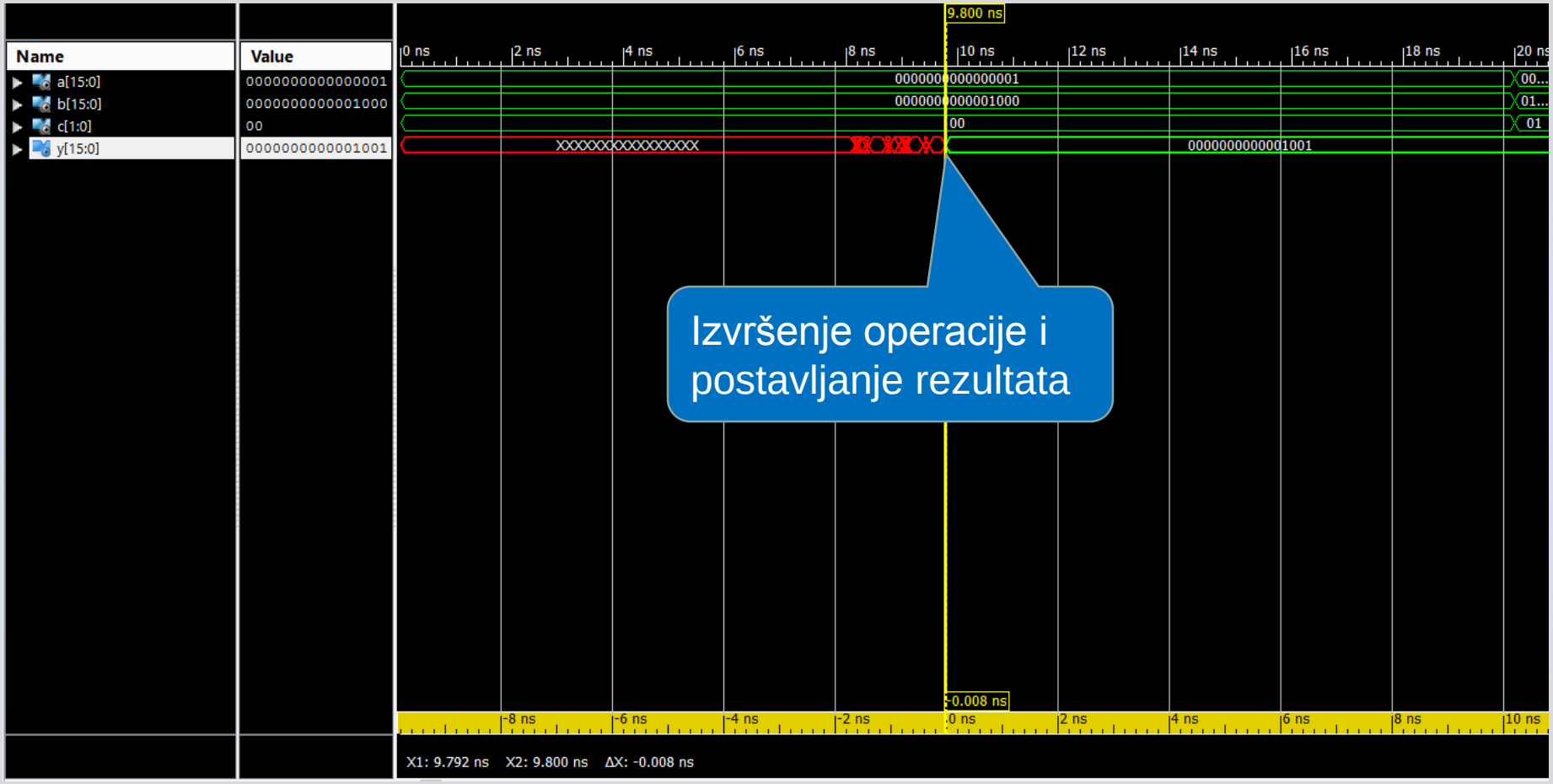


Simulator

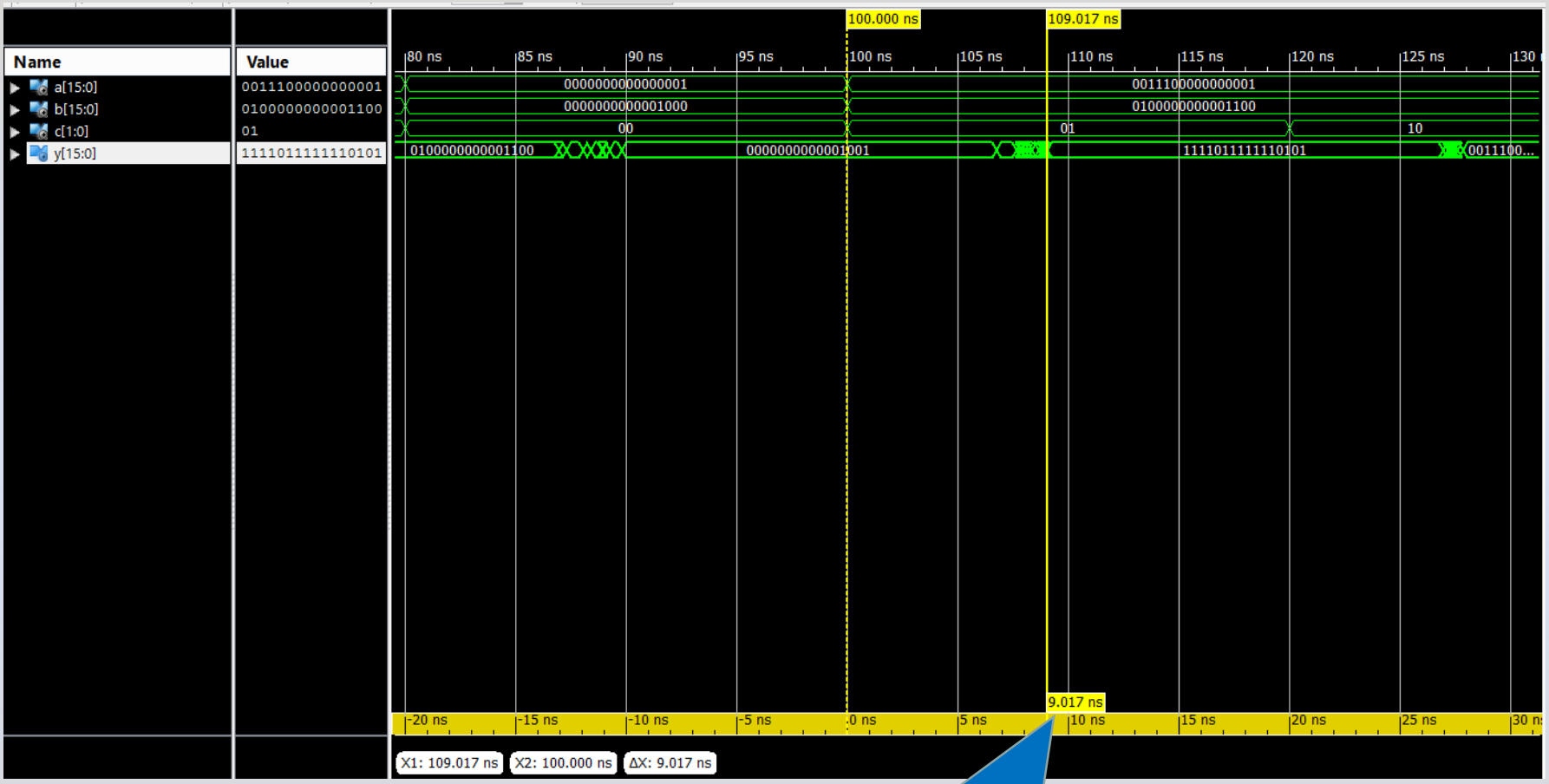
1. Zoom



Simulator

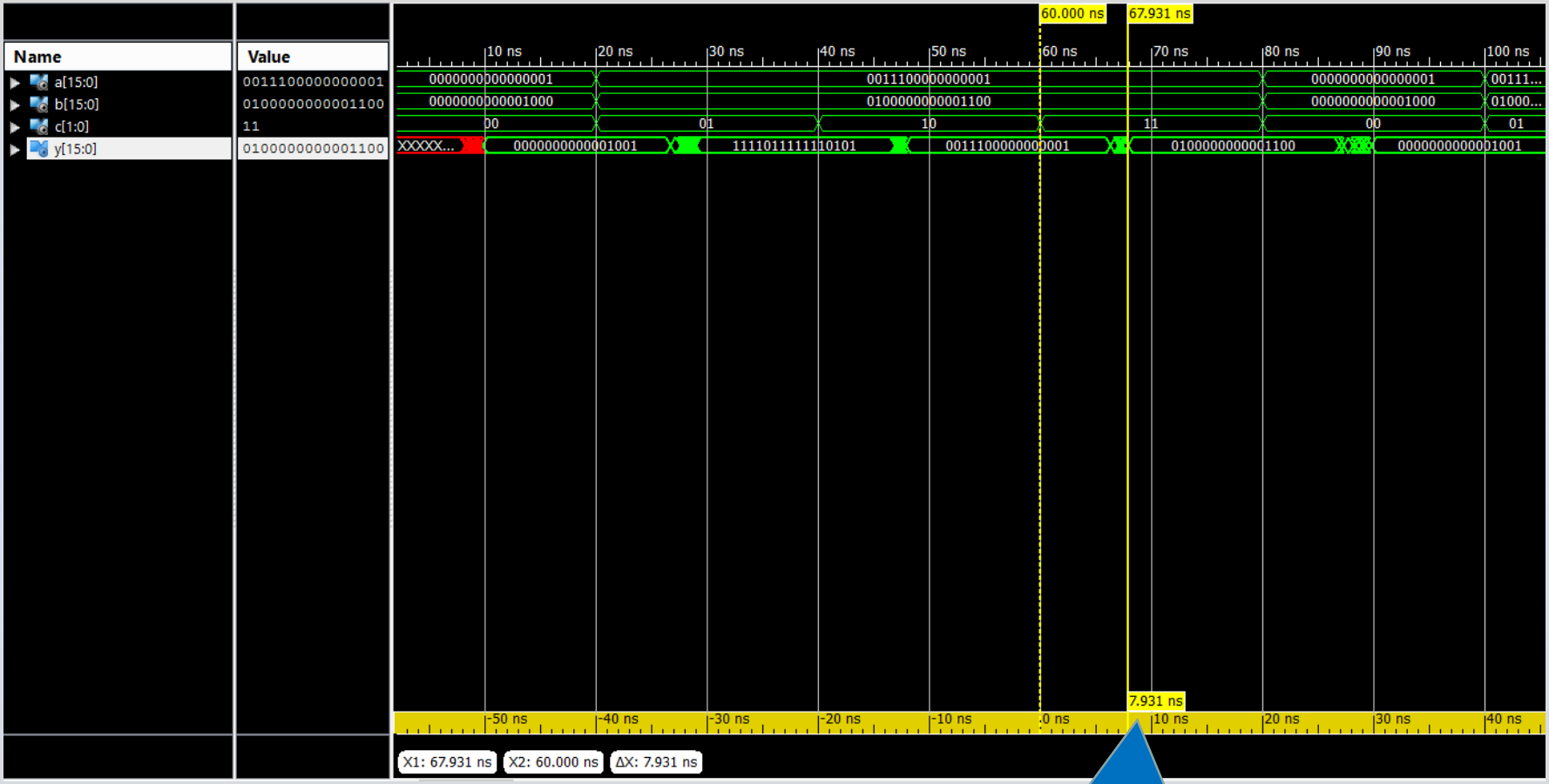

Name
Value
a[15:0]
0000000000000001
b[15:0]
0000000000001000
c[1:0]
00
y[15:0]
0000000000001001
9.800 ns
0 ns
2 ns
4 ns
6 ns
8 ns
10 ns
12 ns
14 ns
16 ns
18 ns
20 ns
0000000000000001
0000000000001000
00
01
xxxxxxxxxxxxxxxx
0000000000001001
-0.008 ns
-8 ns
-6 ns
-4 ns
-2 ns
0 ns
2 ns
4 ns
6 ns
8 ns
10 ns
X1: 9.792 ns
X2: 9.800 ns
ΔX: -0.008 ns
Izvršenje operacije i postavljanje rezultata

Simulator



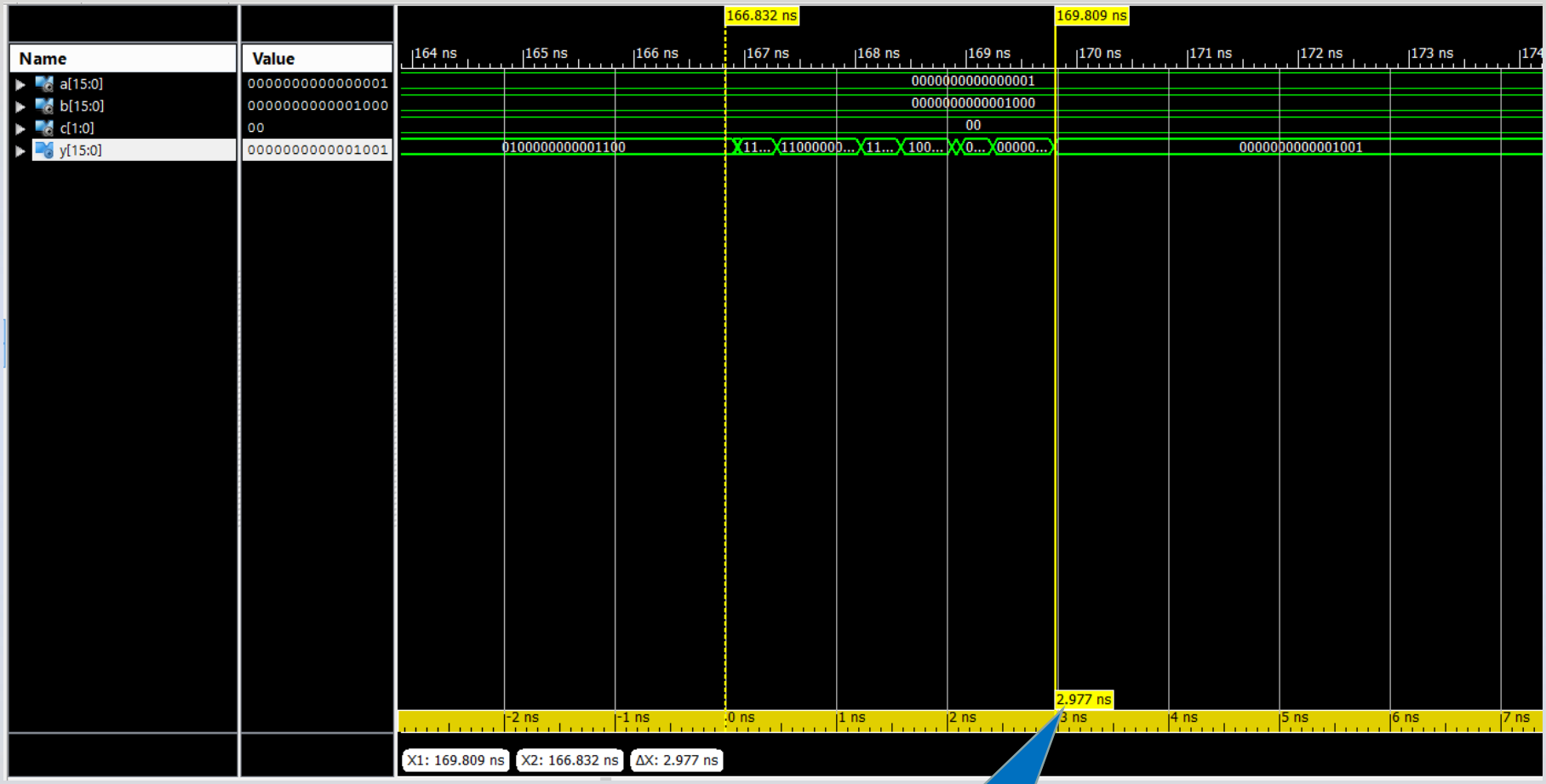
Kašnjenje od trenutka promene jednog od operanada

Simulator



Kašnjenje od trenutka promene tipa operacije

Simulator



Postavljanje rezultata